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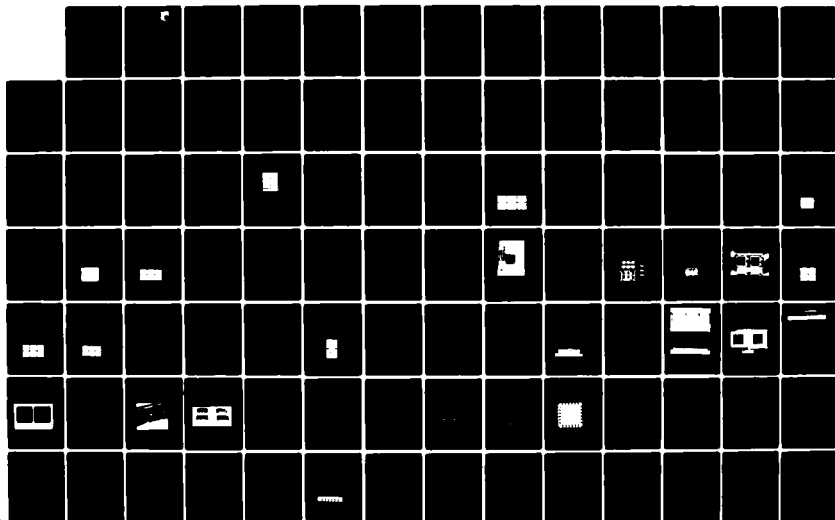
LEADLESS CHIP CARRIER PACKAGING AND CAD/CAM-SUPPORTED  
WIRE WRAP INTERCONN..(U) MAYO CLINIC ROCHESTER MN  
SPECIAL PURPOSE PROCESSOR DEVELOPMEN.. B K GILBERT

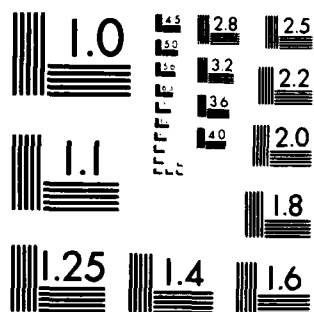
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LEADLESS CHIP CARRIER PACKAGING  
AND CAD/CAM-SUPPORTED WIRE WRAP INTERCONNECT TECHNOLOGY  
FOR SUBNANOSECOND ECL

Mayo Clinic/Mayo Foundation  
Special Purpose Processor Development Group  
Biodynamics Research Unit  
Rochester, Minnesota 55901

NOVEMBER 1981

Interim Report for Period July 1, 1980, through June 30, 1981

Approved for public release; distribution unlimited

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This technical report has been reviewed and is approved for publication.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This document is the second year interim report for a four-year program to refine and develop Computer-Aided Design protocols for implementation of subnanosecond Emitter Coupled Logic in High-Speed Computer Modules using a wirewrap interconnection medium. The software and user manual for implementation guides are not part of the actual report.  This report describes the results of work conducted in the second year of a four year program to develop rapid methods for designing and prototyping		

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## 20. ABSTRACT (Continued)

high-speed digital processor systems using subnanosecond emitter coupled logic (ECL). The second year effort was divided into two separate sets of tasks. In Task 1, described in Sections II-VIII of this report, we have begun a conversion of the design rules, interconnection protocols, special components, and standard logic panels developed during Year 1 for high-speed ECL-based digital processors from a technology based upon dual-in-line packages (DIP) to a technology based upon specially design leadless ceramic chip carriers. This conversion has been undertaken since it was learned during Year 1 that the DIP packages themselves are compromising the maximum performance levels of which the ECL dice are capable. In addition, we have undertaken an extensive investigation of several possible approaches to increasing these operational maxima to an even greater extent than with our present design for new Leadless Ceramic Chip Carriers. Task 2, described in Section IX of this report, was to continue development of a comprehensive computer-aided design/computer-aided manufacturing (CAD/CAM) software package which would be specifically tailored to support the peculiar design requirements of processors operating in a high clock rate, transmission line environment. The CAD/CAM software package has been structured to be sufficiently flexible to assimilate advances in device and component technology, and to accept new sets of design rules resulting from advances in engineering design practice. It is our intention that this CAD/CAM capability will continue to grow in sophistication during the next two years of the project, gradually incorporating operator-interactive design aids which will allow hierarchical block-level design extending down to and encompassing the integrated circuit level.

## FOREWORD

This interim report summarizes work performed under the second year of Contract F33615-79-C-1875 from the Air Force Avionics Laboratory to develop fabrication and design protocols, appropriate components and materials, as well as computer-aided design software, to allow rapid fabrication of prototype special-purpose processors based upon high-speed subnanosecond emitter coupled logic (ECL). This work has been performed by members of the Special-Purpose Processor Development Group, Biodynamics Research Unit, Mayo Clinic/Mayo Foundation, Rochester, Minnesota, and has been administered by the Air Force Avionics Laboratory, Wright Patterson Air Force Base, Ohio, Mr. William A. Anderson (AFAL/AADE-3), Contract Monitor.

The report was submitted by the authors on November 1, 1981, and covers the interim report period from July 1, 1980, through June 30, 1981. The work was performed under the principal investigator, Barry K. Gilbert, Ph.D., Director of the Special-Purpose Processor Development Group, Mayo Clinic/Mayo Foundation. The following members of the Special-Purpose Processor Development Group have both participated in the performance of the work under this project, and have also assisted in the preparation of the text and figures in the body of this report:

D. J. Schwab: Leadless Chip Carrier and Packaging Design  
T. M. Kinter: Computer-Aided Design Software  
K. M. Rice: Computer-Aided Manufacturing Software  
J. M. Dubin: CAD/CAM Demonstration Circuit Design, Fabrication, and Test  
L. M. Krueger: ECL Design Protocols  
R. D. Beistad: Engineering Demonstration Test Circuit Design and Checkout  
S. V. Colvin: Drafting, Fabrication, and Circuit Test

Subsequent interim reports under this contract will discuss continuing efforts to convert to encapsulation of ECL in leadless ceramic chip carriers, and to expansions of the computer-aided design software to support hierarchical system design using large configurable gate arrays fabricated with emitter coupled logic (ECL) device technology.

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## SECTION I

### INTRODUCTION

The Special-Purpose Processor Development Group, Mayo Foundation, Rochester, Minnesota, is developing software and hardware capabilities to support the rapid fabrication in a laboratory prototype environment of ultra-high-speed processors employing system clock rates above 100 MHz. This project has required advances in the use of subnanosecond emitter coupled logic (ECL) components, transmission line design rules, and in the development of new packaging and logic board design and fabrication techniques suitable for high frequency systems. It has also been necessary to prepare new computer-aided design and manufacturing (CAD/CAM) software packages which incorporate the design rules for high frequency transmission line oriented systems.

All of the techniques developed in this project are oriented to the design, fabrication, and testing of new architectures in a system prototyping, not a mass production, environment; hence, design and manufacturing approaches or special equipment unsuitable to the fabrication of one-of-a-kind or prototype processors with a rapid design cycle have been avoided. For these reasons, we have adopted and refined fabrication techniques based upon a modified wire wrap technology, and have avoided the use of multi-layer printed circuit boards designed for a single function. In

this manner, a few types of universal logic boards can be designed and "stockpiled" until needed, then quickly wired and placed into service. The time scales toward which we are working, when all planned design tools are in place, is design durations for systems of moderate size (several thousand integrated circuits) on the order of three months, fabrication cycles on the order of one month, and initial testing durations on the order of three months. By this admittedly ambitious measure, complete development of a processor of moderate size would require on the order of six to seven months. Achievement of such a capability, for processors to operate at clock rates of up to two hundred MHz, will require continuing improvements in a number of tools and technologies.

In the first section of this report, several of the results and the conclusions of our Year 1 Interim Report will be reviewed; new data which was not in final form at the time of the Year 1 report will be presented. The manner in which the conclusions of the Year 1 studies have motivated the work carried out during the second year of this project, much of which will be continued in Project Year 3 now commencing, will also be described.

## SECTION II

### REVIEW OF YEAR ONE RESULTS AND EFFORTS MOTIVATED FOR YEAR 2 BY THESE RESULTS

#### 1. Performance of ECL, TTL, and Other Logic Families

##### a. Speed Performance Comparisons

The performance improvements inherent in high-speed digital device technologies can be exploited in a variety of design tradeoffs and compromises. For example, either a very high throughput can be obtained for a given number of components, or conversely, a desired throughput can be achieved with fewer subprocessors and/or pipeline stages, since each component can execute a very large number of operations per second. Before initiating the development of a new processor, designers of new systems should, but usually do not, seriously review the available types of digital device technology. Such a review should include the low power metal oxide semiconductor (MOS) technologies and the conventional and enhanced speed versions of transistor-transistor logic (TTL). In addition, consideration should be given to several modern families of ultra-high-speed logic which rely upon low impedance transmission line interconnects, low logic swings, and subnanosecond gate delays and risetimes. Presently, emitter coupled logic (ECL) and current mode logic (CML), both fabricated with silicon technology, both belong to the class of transmission line logic families; in the future, devices relying upon the material and

electrical properties of gallium arsenide and perhaps indium phosphide are also likely to become available.

Modern emitter coupled logic components demonstrate considerable speed advantages over the more familiar TTL families, both on a per-gate basis for logic and arithmetic elements, and in decreased cycle times for static random access memory. Although there has been considerable reluctance by designers to confront new device technologies with subnanosecond propagation delays and risetimes, which require the use of transmission line concepts for interconnections between components, the order-of-magnitude throughput enhancement possible with these devices in comparison to TTL is well worth the effort if a high performance design is required.

In those instances in which the complexity of a processor can be decreased by using higher speed logic families, an additional operating benefit is achieved. In general, the mean time to failure of a given system is roughly proportional to the number of individual integrated circuits, and particularly to the number of interconnects between these devices; the number of interconnect-related failures is frequently three to five times that of the number of component-related failures. Conversely, and provided that proper design, fabrication, and test protocols are employed, the mean time to failure of a system is not significantly affected by increases in the system clock rate or decreases in the component gate

propagation delays. Hence, a well designed system which achieves a given throughput by an exploitation of high-speed device technology will demonstrate improved mean times to failure in comparison to a system employing slower clock rates and a large number of integrated circuits to achieve the same throughput. In those instances in which extremely high computational capacity is required, both parallelism and high throughput for individual components are requisites of system design.

#### b. Power Dissipation Comparisons

It is commonly believed that ultra-high-speed components such as emitter coupled logic consume too much power and require too much cooling to be used in conventional systems. The reality of the situation is much more complex, as may be observed in Figure 1, which depicts the relationships between average power dissipated per gate for a number of different logic families as a function of system clock rate. Low power complementary MOS (CMOS) logic, low power Schottky TTL, and several families of emitter coupled logic (including the now obsolescent family Motorola MECL III) are compared in this figure. In addition, the so-called dynamic switching energy of the particular logic family is presented as an auxiliary parameter. Dynamic switching energy, stated in joules, is the product of the gate power,  $P_D$ , and the gate propagation delay or switching delay,  $T_d$ . For many types of digital logic, both

# POWER REQUIREMENTS OF VARIOUS LOGIC FAMILIES AS FUNCTION OF SYSTEM CLOCK RATE

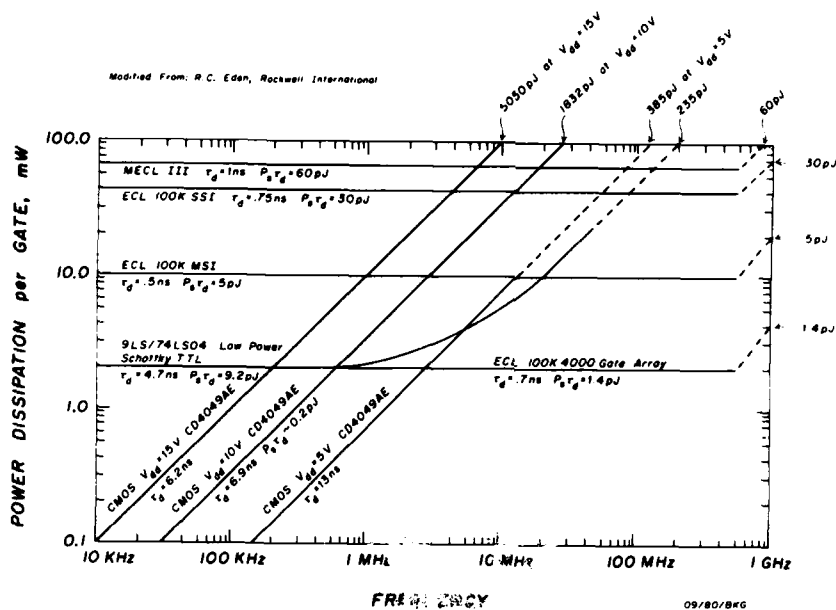


Figure 1

the gate power and the switching energy remain relatively constant over the lower range of clock frequencies, but then increase logarithmically above a specific clock frequency which is characteristic of each logic family. Though not presented in this figure, conventional and Schottky TTL display similar behavior, with the curve for Schottky TTL located above and to the left of the curve for low power Schottky TTL. This increase in average gate power with increasing clock rate results from the internal design of the output transistor structures in the MOS and TTL components, which exhibit a structure of paired transistors connected in series between the power supply and ground, as depicted in Figure 2 for a typical high-speed (H)

TTL gate. For a short duration during the switching transition, both the upper and lower transistors  $T_4$  and  $T_5$  in the output structure are biased into their conducting region, creating a low impedance, high current path between the power bus and ground.

Conversely, Figure 1 shows that the various families of emitter coupled and current mode logic exhibit essentially constant power dissipation regardless of clock rate. Constancy of power dissipation results from the design characteristics of the internal ECL gate, as depicted in Figure 3. The emitter coupled and current mode logic gate structures employ transistors operating in parallel, complementary pairs, with complementary logic levels; the amount of current flowing through each gate is maintained at a constant value by a current source and is balanced between at least two transistors (for example, between the transistor pair  $T_{1A}/T_{1B}$  and transistor  $T_2$ ); when the gate polarity is switched, one of these transistors ( $T_{1A}$  or  $T_{1B}$ ) moves towards (but not into) its cut-off region by the same amount as the complementary transistor ( $T_2$ ) moves towards its saturation region; at no time, either within or outside the transition region of the gate, does a low impedance pathway exist between ground and the power bus. In addition, since the transistors are never allowed to approach either their saturation or cutoff regions, the gate switches rapidly and presents a more or less constant current drain to the power supply during all phases of its operation. If output transistors are employed

to drive signals to another component, they are also configured in complementary pairs (e.g.,  $T_3$  and  $T_4$  in Figure 3). As a result of this operational behavior, it may be observed from Figure 1 that above a specific frequency which is characteristic

**BASIC SWITCH STRUCTURE EMPLOYED IN  
HIGH-SPEED SERIES 74H TTL GATE**

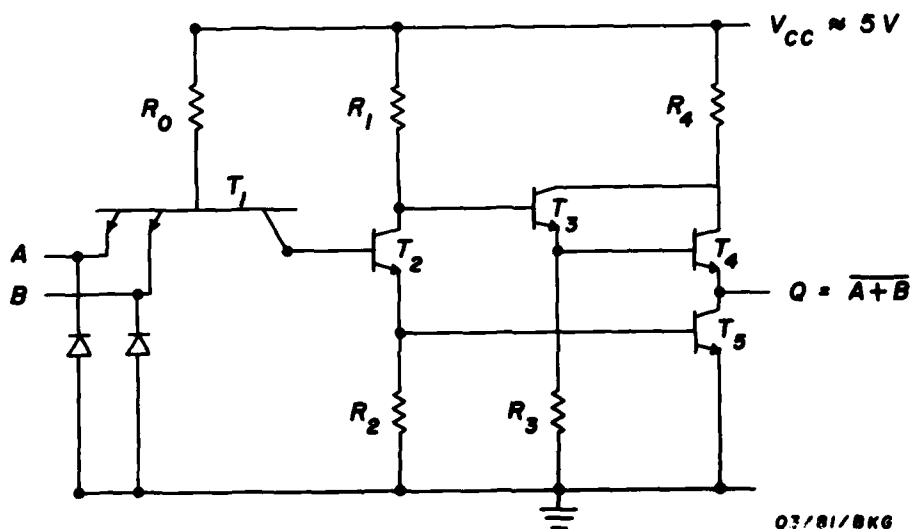


Figure 2

Basic switch structure used in a high speed series 74H TTL NOR-gate. When either A or B are low,  $T_2$  is turned off, which turns  $T_3$  and  $T_5$  off, while  $T_3$  turning on turns  $T_4$  on; Q switches to a logic HIGH.  $T_4$  and  $T_5$  are in a "totem pole" configuration and are high-power transistors. Currents through  $T_4$  and  $T_5$  change drastically when the gate switches states.

of the logic families being compared, the more modern families of subnanosecond emitter coupled logic (ECL) are more conservative of power and require a lower switching energy than either the MOS or TTL devices. This frequency is approximately 11 MHz for CMOS with the supply voltage at 5V, and approximately 18 MHz

### BASIC SWITCH STRUCTURE EMPLOYED IN SUBNANOSECOND ECL GATE

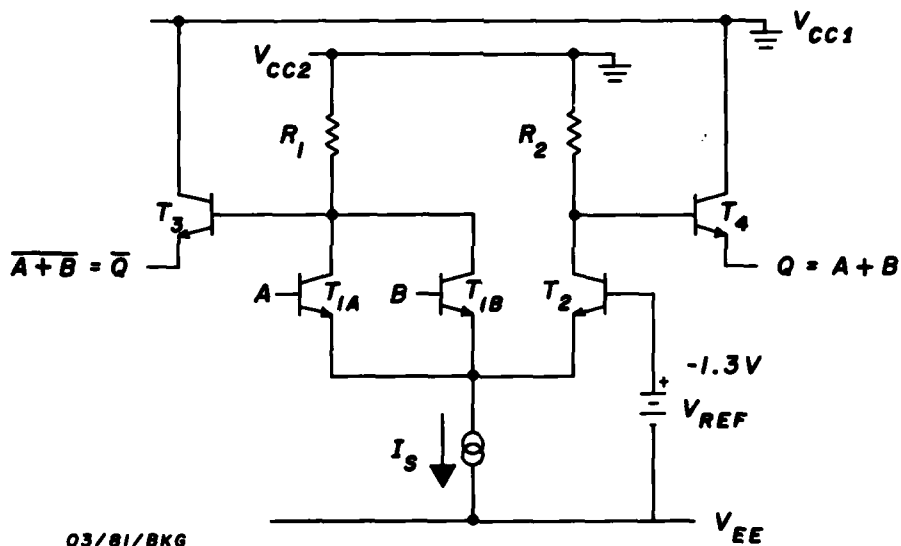


Figure 3

Basic switch structure used in an ECL gate. The sum of currents through transistors  $T_{1A}$  and  $T_{1B}$  and  $T_2$  is always constant. Likewise, if  $Q$  and  $\bar{Q}$  are both terminated in the same impedance, the sum of the currents through  $T_3$  and  $T_4$  is a constant.

for low power Schottky TTL in comparison to the subnanosecond ECL medium scale integrated circuit (MSI) gates. Figure 1 also indicates that considerable progress has been achieved in decreasing the gate power of successive generations of emitter coupled logic, from the 60 milliwatt gate dissipation of the Motorola MECL III introduced in 1968, to the two milliwatt gate dissipation of the most modern Isoplanar S subnanosecond ECL gates introduced in early 1981. Much of the poor regard in which ECL is held is based upon unfortunate experiences with the 1968 technology which are no longer valid. Finally, although the development of logic families based upon gallium arsenide is in its infancy, the gate level design of GaAs digital components should also employ complementary transistor pairs; if this approach is adopted, the power dissipation of gallium arsenide components will also be constant regardless of operating frequency and will exhibit very much lower gate power dissipation and switching energy than silicon devices; gallium arsenide may thus become a very attractive technology for the implementation of ultra high-speed systems.

#### c. Device Density and Clock Rate/Density Comparisons

The high speed logic families have also been criticized for an inability to achieve levels of single component integration to LSI (300-3000 gates) or VLSI (3000 gates and above) densities while still maintaining short propagation delays

and short output risetimes. Although the MOS technologies in particular have demonstrated more rapidly increasing gate density per year than have the bipolar technologies (MOS integrated circuit complexities of 25,000 gates have recently been reported by a Control Data/Westinghouse team), advanced bipolar fabrication techniques will also support high gate densities. For example, a 16 K-bit x 1 static random access memory component under development in the first quarter of 1981 is an ECL device; in addition, several high complexity arithmetic and logic components presently in design by Fairchild Camera and Instrument Corporation employing well established ECL fabrication methods are achieving 1,000-2,000 gate density in mid-1981; lastly, bipolar components fabricated with an advanced process technology were reported by Honeywell in early 1981 with gate densities of 3,000-10,000 gates and subnanosecond propagation delays and risetimes.

The functional throughput rate (FTR) of a device technology is defined as the product of the number of gates on an individual integrated circuit and the effective clock rate at which these gates can be operated, divided by the area of the chip in  $\text{cm}^2$  (FTR is thus stated in units of gate hertz/ $\text{cm}^2$ ). The high density MOS device technologies maximize FTR by increases in the number of gates per  $\text{cm}^2$  at the expense of clock rate; conversely, the current mode logic families such as ECL maximize FTR with a moderate gate density but extremely high clock rates. For example, the best commercial low speed

high density microprocessor components have exhibited functional throughput rates of up to  $10^{11}$  gate-hertz/cm<sup>2</sup>, whereas the FTR of the newest ECL components presently exceeds  $5 \times 10^{11}$  gate-hertz/cm<sup>2</sup>, with 7000 gate density and clock rates greater than 100 MHz, as recently reported by Honeywell, Inc. In a number of applications, particularly those in which real-time on-line processing of high digital rate data must be achieved, at least a portion of the processor must operate at extremely high clock rates. For example, if data from returned radar signals is sampled every ten nsec, at least a portion of the processor will have to operate at a 100 MHz clock rate until the data stream can be parallelized and the equivalent clock rate reduced to lower levels.

#### d. The Component Interconnect Problem

In spite of the trend toward increasing gate densities on each integrated circuit, the interconnect problem between such integrated circuits remains, and is in fact becoming more critical. The following comments will attempt to place the component interconnect problem into perspective. Among the numerous reasons cited for the attempts to increase on-chip density are 1) minimization of the number of interconnects, thereby decreasing the number of failure points in a system; 2) throughput improvements resulting from the short propagation delays between on-chip functions versus the much larger propagation delays in functions located on multiple integrated

circuits; and 3) improvements in the packing density of the completed processor. However, improvements in the performance characteristics of modern families of digital integrated circuits indicate that internal gate propagation delays even of the slowest MOS devices will decrease to much less than 2 nsec, while the most advanced bipolar gate structures are already exhibiting internal gate propagation delays in the 200-400 psec range. Hence, the time lost in the communications pathway between integrated circuits will become increasingly detrimental to overall system operation if measures are not taken to decrease these delays as well. For example, as the internal propagation delay of a "typical" gate approaches 1 nsec, presently employed "typical" TTL output risetimes of 5 to 10 nanoseconds will squander the equivalent of 5 to 10 internal gate delays as the signal is driven between integrated circuits.

It has been frequently stated that interconnect lengths between individual integrated circuits are rapidly becoming the major impediment to enhanced system performance; however, many signal processor designs which exploit pipelining and parallelism employ a flow-through design. That is, architectural feedback path lengths are minimized and the individual operations are moved successively from one physically adjacent section of logic to another. The propagation speed of a wavefront along an interconnect varies between 1 and 2 nanoseconds per foot; appropriate layout of logic sections generally minimizes the physical distance between processor elements to several feet or less, and in many cases to a few inches. An

intercomponent signal risetime of 5 nanoseconds dissipates as much time as nearly 3 feet of interconnect, a relatively long distance considering the improvements in system packing density achieved in recent years. Although it is definitely true that the intercomponent separations must be maintained at minimum lengths, it is also true that considerable effort should be expended to achieve short intercomponent signal risetimes.

The attainment of short intercomponent risetimes can be accomplished in two ways. The interconnect protocol can require that all signal pathways be treated as transmission lines, with appropriate matched impedance terminations placed at one or both ends of the line; alternately, the interconnects can be treated as conventional wire runs with no special consideration of their transmission line behavior. Examples of both protocols are widely extant. Recognizing the importance of short output risetimes, designers of Schottky TTL and subnanosecond ECL devices have addressed this problem in different ways and with quite different results. As depicted in Figure 4, the risetime of the Schottky gate is approximately one nsec but is intended to be driven into unterminated interconnects whose electrical characteristics are not controlled; i.e., the interconnect is not treated as a transmission line. However, the interconnect nonetheless behaves as a transmission line when confronted with short risetime signals (of one nsec or less) whether or not it has been designed as a transmission line.

To a first approximation, if the interconnect is of a sufficient length that the round trip signal propagation time between the source gate and the most distant destination and back to the source is less than the risetime of the signal, the inherent transmission line nature of the interconnect may be disregarded; conversely, if the risetime of the signal is approximately equal to or considerably less than the round trip propagation time, the transmission line characteristics of the interconnect will play a significant role in signal behavior, and hence in system behavior. For purposes of discussion, assume an interconnect whose inherent propagation delay is 1 nsec per foot and a typical signal risetime of 0.5 nsec, as is the approximate case for subnanosecond ECL gates. In such a case, all interconnects would have to be less than 3 inches in length for the designer to safely disregard the transmission line characteristics of the interconnects. Since it is difficult in practice to guarantee all interconnect lengths in a processor to be less than 6 inches, much less 3 inches, the transmission line behavior of the interconnects should be accommodated whenever a logic family is employed with characteristic risetimes of one nsec or less.

When the designer fails to account for the transmission line characteristics of the system interconnects, the consequences are usually readily apparent. The upper two panels of Figure 4 depict the rise and falltimes of a typical Schottky TTL gate driving a single receiving gate through a two inch

of to-and-fro reflected wavefronts will traverse the line through several complete cycles of gradually decreasing amplitude; the average voltage on the line gradually approaches the

WAVEFORMS RECORDED FROM DIGITAL PROCESSOR  
FABRICATED WITH SCHOTTKY TTL COMPONENTS  
(14.3 MHz System Clock; Ground/Power Plane Logic Boards)

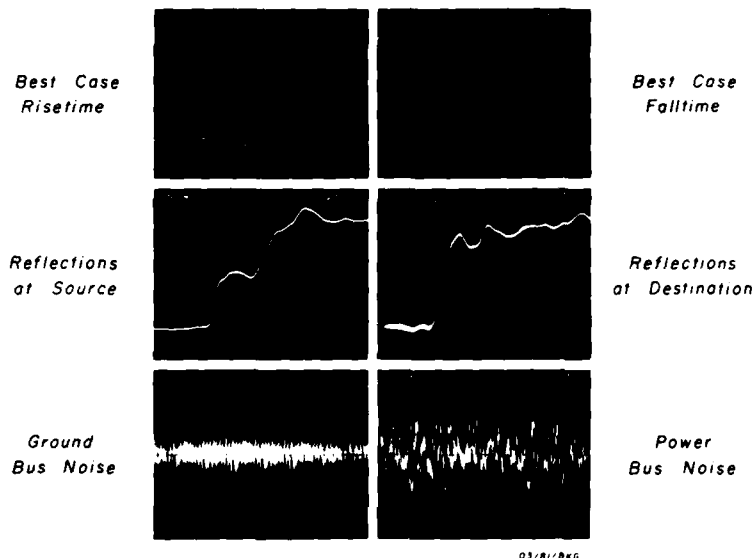


Figure 4

Behavioral characteristics of a processor system fabricated with Schottky TTL components. Note the one nsec risetimes and falltimes of the output gates (upper panels), creating multiple reflections on the unterminated interconnect lines (middle panels); note also the large amount of noise on the power bus and ground bus (lower panels) resulting from the unbalanced current drains caused by the totem-pole, asymmetrical design of the Schottky TTL gates.

interconnect; in both cases, the measuring probe was placed at the source. Note the approximately one nsec risetime and fall-time of the wavefront, which propagates down the interconnect at a rate, usually 1-2 nsec/foot, which is characteristic of the insulating material and physical separation between the signal line and ground. When the propagating wavefront reaches the far end of the line, it is reflected back toward the source with the same polarity as the impinging wavefront if the apparent impedance at the end of the line is greater than that of the line, and conversely.

In a TTL environment, the input impedance of a Schottky TTL gate is in the neighborhood of 20,000-40,000 ohms shunted by 10-20 pF, in comparison to a characteristic impedance of the interconnect in the range 50-300 ohms. For input signals with one nsec risetimes and high frequency components, the interconnect thus behaves as a transmission line which is virtually short circuited at its far end due to the low impedance effects of the shunt capacitance of the Schottky gate input circuit. From transmission line theory, it can be predicted that when the impinging wavefront reaches the end of the line, a massive voltage reflection wavefront of opposite polarity will propagate back toward the source. When this secondary wavefront approaches the source gate, it is again reflected, since the output impedance of the source gate is unequal to that of the line (usually 10-20 ohms in the low state and 350-400 ohms in the high state of the TTL gate). This sequence

desired logic level. Since these to-and-fro reflections cause the instantaneous voltage at the inputs of destination gates on the signal string to approach and recede from the threshold level in an unpredictable manner, enough time must be allowed for the line voltage to stabilize before the input voltage on any receiving gate will be in the same state as that of the driving gate (Figure 4, middle panels).

An additional problem, alluded to in a prior paragraph, is that the noncomplementary nature of the gate design of TTL components causes large switching currents to be drawn from the power bus following each clock transition. Since the power supplies themselves cannot respond to these changes in current demand rapidly enough, the instantaneous voltage on the bus of a system fabricated with TTL decreases momentarily and then rises back to its initial value. These rapid fluctuations in the supply voltage are observed by each component as power bus noise, which degrades the overall noise immunity of the system. This behavior is clearly visible in the lower panels of Figure 4, which show the power bus noise and the ground bus noise in a typical Schottky TTL system operating at a clock rate of only 14.3 MHz. The amplitude of the bus noise usually becomes much greater with increasing clock frequency in TTL systems, because successive noise spikes add algebraically due to insufficient decay times between pulses.

Conversely, if the integrated circuits and their respective output gates are designed from the outset for a low impedance

transmission line environment, with all interconnects terminated in their characteristic impedance, many of the problems described in the preceding paragraphs are alleviated. When an impinging wavefront reaches the end of a transmission line terminated in its characteristic impedance, no primary or secondary reflections occur whatsoever; the state of the line stabilizes immediately at the level to which it was switched by the driving gate. The receiving gates on the line observe a stable logic level at their inputs after a single propagation delay duration between the driving gate and the farthest receiving gate on the string. Hence, the logic can be clocked at a rate limited only by the across-component and intercomponent propagation delays, without regard for line settling requirements.

The combination of low impedance terminated transmission line interconnect protocols and digital components exhibiting small logic voltage swings and balanced internal gate designs possesses several operational advantages in addition to their freedom from reflections. Components generating logic swings of only 700-800 mV and risetimes in the 500-600 psec range create less than half the crosstalk voltage levels between interconnects as those logic families whose risetimes are approximately one nsec and whose logic swings are several volts, though a detailed justification of this statement is beyond the scope of this report. In addition, the use of logic gates

whose design employs balanced, complementary transistor structures, such as the various families of ECL, create rather small instantaneous changes in current drain from the power busses. These operating characteristics explain in large measure the good results presented in the Year 1 Interim Report, which are presented again here for completeness. Figure 5 depicts measurements from an ECL system operating at a clock rate of 125 MHz (nine times greater than the TTL system of Figure 4), with optimally terminated transmission line interconnect protocols; the current drain from the power busses is balanced at all times because of the design of the ECL gates. Rapid intercomponent communications unencumbered by reflections, crosstalk, and

**DIRECT CONVOLUTION FILTER PROCESSOR  
FABRICATED WITH SUBNANOSECOND ECL**  
(125 MHz System Clock; 6-Bit Input and 18-Bit Output Data;  
9 Elements; Wire Wrap Interconnects)

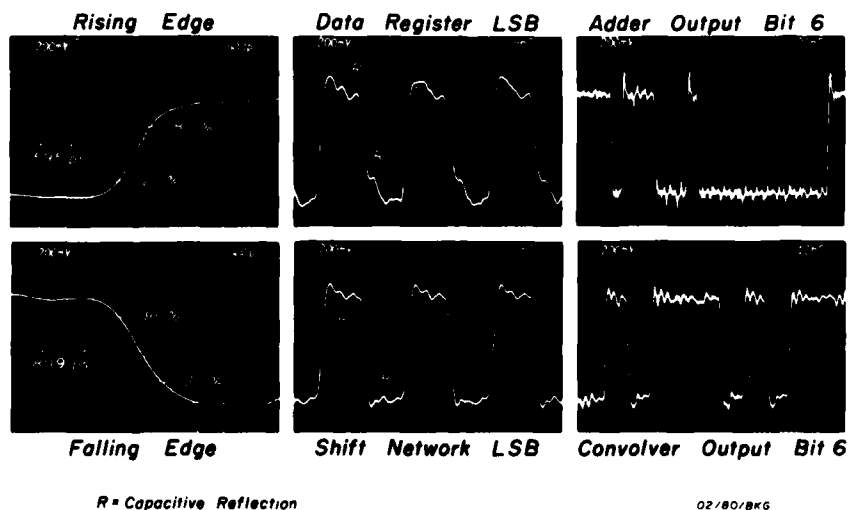


Figure 5

power supply noise can thus be achieved by the use of low impedance transmission line interconnect protocols, in conjunction with a family of digital logic designed to minimize fluctuations in current drain on the power bus.

e. Costs of System Fabrication with Transmission Line  
Logic Families

Although there is at present a small cost penalty for system fabrication with transmission line logic families, these penalties have been overstated. The performance improvement gained and the cost penalties incurred by such an approach are illustrated by a recent design study performed in this laboratory for an interconnect network to be used with multiple independent communicating processors. In such a structure, data packets are transferred between successive data registers connected one to another in a closed-ring topology. Each uniprocessor on the network communicates with its companion processors by transferring data into its associate local ring register, formatted with an appropriate destination address; the entire data packet is placed on and then transferred around the ring until it reaches the appropriate destination, where it is removed from the ring by the processor to which it is addressed. The register on the ring associated with each processor and the ancillary logic necessary to place a data element on the "ring", or remove a data item from the "ring" for any given processor is called a ring node. A baseline design study was

carried out for three logic families: low power Schottky TTL, Schottky TTL, and subnanosecond ECL; only commercially available SSI, MSI, and LSI components were employed in the study. The engineering effort and the component, logic board, and materials costs to fabricate a ring node in each technology, as well as the maximum data transmission capability of a node, were assessed for each of the three device technologies (Table 1). The ECL technology illustrates a substantial performance advantage over either of the TTL technologies investigated. The relative costs of manufacturing a typical ring node and the relative performance/cost ratios of the three technologies and two word widths (millions of words transferred per second divided by cost per node) were also investigated. For all cases examined, though approximately 5 percent more expensive than their equivalent Schottky or low power Schottky TTL equivalents, the ECL designs achieve considerably higher throughput and considerably improved performance/cost ratios. Several similar studies for other types of systems have confirmed these results.

f. Review of Performance Limitations Detected in DIP-  
Encapsulated Subnanosecond ECL

As reported in detail in the Year 1 Interim Report, this laboratory has demonstrated that the subnanosecond ECL dice encapsulated in either ceramic or plastic dual in-line packages are incapable of operating at clock rates in excess of 250 MHz,

TABLE 1

DATA TRANSFER CAPACITY, RELATIVE COST, AND  
PERFORMANCE/COST OF RING NETWORK COMMUNICATIONS NODE  
FOR DIFFERENT DIGITAL DEVICE TECHNOLOGIES

Device Technology	Low Power Schottky TTL	Schottky TTL	Subnanosecond ECL
Data Transfer Rate, Megaword/sec (Worst Case)	5.5	9.2	51.0
Relative Performance	1	1.67	9.27
Relative Cost, Protocol 1 <sup>+</sup>	1	1.02	1.09
Relative Cost, Protocol 2 <sup>°</sup>	1	1.02	1.06
Performance/Cost, Protocol 1 <sup>+</sup>	1	1.64	8.50
Performance/Cost Protocol 2 <sup>°</sup>	1	1.64	8.75

<sup>+</sup> 16 Bits Data, 24 Bits Local Address, 8 Bits Node Address =  
48 bit word

<sup>°</sup> 32 Bits Data, 24 Bits Local Address, 8 Bits Node Address =  
64 bit word

in spite of the fact that many of the part types are rated to 500-550 MHz clock rates. Through a series of tests, the results of which are summarized in the following paragraphs, it was possible to demonstrate that the speed limitations are imposed not by the logic board and wire wrap technology developed in the Mayo Foundation Year 1 research, but solely by the DIP encapsulation. Further, as demonstrated by the following results, conversion of the packaging technology from one based upon dual in-line packages to one exploiting appropriately designed leadless ceramic chip carriers (LCCC), will make available nearly the maximum performance of which the dice are capable.

3. Performance at 1 GHz and 2.5 GHz Clock Rates of Special ECL Components Interconnected With a Wire Wrap Protocol

As a verification that the logic panel and wire wrap interconnect protocol described in the Year 1 Interim Report were not responsible for the less than maximum performance of the CERDIP-encapsulated subnanosecond ECL devices, two generations of advanced ECL components fabricated by Fairchild Camera and Instrument Corporation with the new Isoplanar S integrated circuit technology (transistor  $f_T$  values are approximately 7 GHz) were obtained in specially designed miniature dual in-line packages. These special components were installed on the wirewrappable ECL logic panel developed in the Year 1 research, and driven by a clock signal from a commercial clock generator

(see Year 1 Interim Report, pp 91-92). The source clock rate was gradually increased to approximately 1 GHz. Figure 6 shows the results of the first experiment; the lower trace depicts the clock signal, which appears sinusoidal because of the low-pass frequency characteristics (oscilloscope amplitude response is -3 dB at 1 GHz) of the Tektronix 7104 oscilloscope. The upper trace shows the divide-by-four output of the high-speed counter, which operated with no missed transitions. A second experiment was performed in January 1981, using an even more advanced set of experimental components manufactured by Fairchild. The tests documented in Figure 6 were repeated, but the clock frequency was gradually increased to 3.19 GHz before the wire wrapped circuit ceased function, as indicated by sampling oscilloscope measurements (Fairchild predicted the clock rate limitation of the new dice irrespective of package limitations at

HIGH FREQUENCY PERFORMANCE OF ADVANCED-DESIGN  
SUBNANOSECOND EMITTER COUPLED LOGIC (ECL) COMPONENT  
AND WIRE WRAP INTERCONNECT TECHNOLOGY

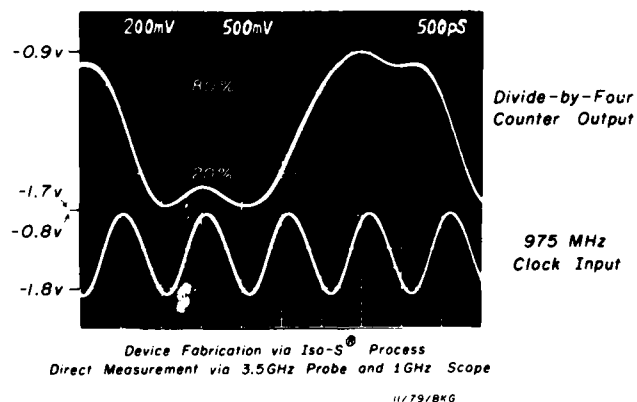


Figure 6

3.3 GHz). Figure 7 shows the results of direct measurement on the circuit with a Tektronix Model 7104 oscilloscope at 2.5 GHz, the maximum direct recording frequency of the Tektronix 7104. These results indicate that the wire wrap board and interconnect technology are capable of supporting clock rates well in excess of the 250 MHz maximum rate observed when Cerdip encapsulated ECL dice were employed.

### 3. Circuit Performance Improvements Obtained With Leadless Chip Carrier Encapsulation

To investigate the possibility that the subnanosecond ECL dice packaged in leadless chip carriers would demonstrate improved electrical performance, tests were conducted of ECL dice of two generic part types packaged in 24-pin ceramic leadless chip carriers (see Year 1 Interim Report, pp 93-97). A small two layer copper-clad brassboard test circuit was fabricated with lead tab contact spacing to match the padout spacing of the leadless chip carriers; twisted pair interconnects were then bump soldered to the copper clad printed circuit card. A series of time domain reflectometry and operational tests were then undertaken. Reflectometry studies indicated that the total impedance discontinuity for the ECL dice encapsulated in a ceramic leadless chip carrier is considerably less than that for an identical ECL chip packaged in a Cerdip. The leadless chip carrier brassboard was then tested operationally to ascertain whether the maximum achievable

clock rate would exceed the 250 MHz maximum usable frequency observed for the ECL dice in Cerdip packages. The circuit was able to operate correctly up to a clock rate of 454 MHz, the highest usable clock rate for any subnanosecond ECL circuit which we had achieved to that time. The small test circuit, measurements from which are depicted in Figure 8, was fabricated on a crude brassboard without adequate power plane decoupling, and displayed noise characteristics reminiscent of the preliminary dual in-line package brassboard studies conducted early in Year 1 of this project. The waveforms depicted in the four leftmost panels of Figure 8 were considerably "cleaner" than those from test circuits fabricated with Cerdips.

**HIGH FREQUENCY PERFORMANCE OF ADVANCED-DESIGN  
SUBNANOSECOND EMITTER COUPLED LOGIC (ECL) COMPONENT  
AND WIRE WRAP INTERCONNECT TECHNOLOGY**

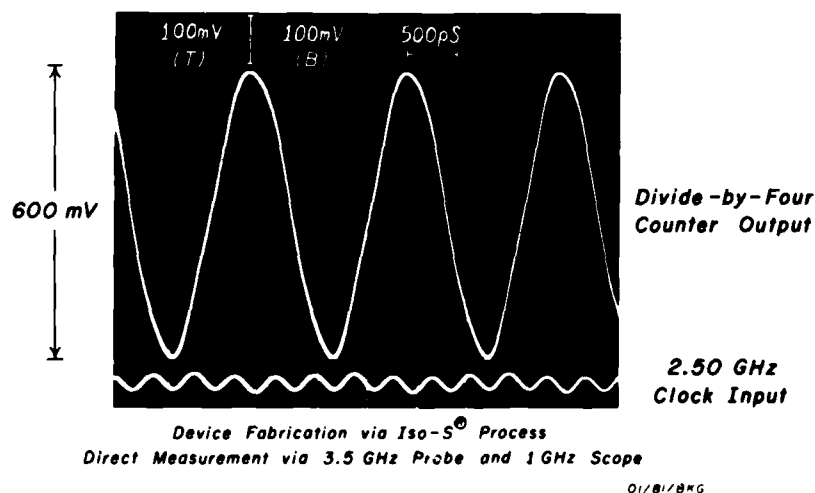


Figure 7

By the end of the Year 1 research it had become apparent from the studies described in the Year 1 Interim Report that the major impediment to achievement of maximum performance from the subnanosecond ECL dice was not the wire wrap protocol, the logic panel design, interwire, or terminator induced cross-talk, or power plane noise, but the internal structure of the ceramic dual in-line packages. It was clear that the only way to exploit the full performance of the high-speed ECL dice would be through the adoption of a new packaging approach characterized by low levels of input shunt capacitance and series inductance within the package, i.e., an encapsulation,

PERFORMANCE CHARACTERISTICS OF PROTOTYPE  
SYNCHRONOUS SUBNANOSECOND ECL CIRCUIT  
EMPLOYING LEADLESS CHIP CARRIER ENCAPSULATION  
(454 MHz System Clock via Square Wave Oscillator;  
Carriers Bump Soldered to PC Board)

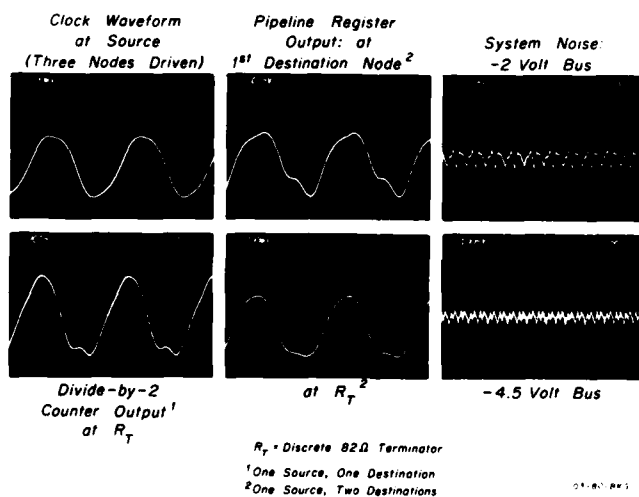


Figure 8

packaging and logic board technology based upon ceramic leadless chip carriers. This is the development effort which was undertaken in the Mayo laboratories as part of the Year 2 research effort.

#### 4. Requirements for Conversion to Leadless Ceramic Chip Carrier Technology

The preliminary tests with commercially available ceramic leadless chip carriers solder bonded to a crude brassboard circuit were encouraging; nonetheless, these tests did not provide sufficient data to commit large amounts of funds and manpower to the development of a new packaging system based upon ceramic leadless chip carriers. More refined tests were required. Accordingly, the development of an improved test vehicle much closer to the final intended designs for a new wire wrap board, terminators, and chip carriers, was undertaken. Provided that these tests of an improved brassboard with commercially available leadless chip carriers did indicate feasibility of the overall project, it would then be necessary to identify a ceramic leadless chip carrier whose electrical and thermal characteristics would be compatible with the subnanosecond ECL dice. First, an appropriate chip carrier would have to dissipate the relatively high levels of power (250 milliwatts to 1 watt) generated by the ECL dice. Second, the short risetime, high-current signal swings (7-15 milliamps) characteristic of these devices mandated that the

chip carrier demonstrate low series inductance and low values of shunt capacitance between the individual signal leads and ground, and between adjacent signal leads. The values of these parasitics selected initially were shunt capacitances of less than 2 pF and series inductances of less than 1 nano-henry; it was not clear that these low values could be attained in practice. Lastly, since the areas of subnanosecond ECL dice presently available or currently envisioned encompasses a range of 7 to 1, either several sizes of leadless chip carrier would be required, or else a single chip carrier with fixed outer dimensions but different die well dimensions would have to be identified. It was also necessary to minimize the number of leadless chip carrier sizes, since optimization of a universal board layout becomes increasingly difficult as the number of package sizes increases. In addition, subnanosecond ECL requires local placement of logical, arithmetic, and memory functions as needed on a logic panel, rather than a grouping of all memory components, all logical components, and so on; only by distribution of functions to the local region of need can the maximum speed performance of the ECL dice be exploited. This design requirement of ECL dice, that functions be contiguous on a logic board to decrease propagation delays, is a unique characteristic of all high-speed devices not normally encountered in the design and development of systems using MOS or TTL logic. This requirement placed an added constraint on the designs of the leadless chip carrier packages.

Next, a suitable design was required for a universal logic panel optimized for the leadless chip carrier to be selected. The new logic panel was envisioned to be multilayer, but with the layers carrying only ground and the two power voltages, -2 volts and -4.5 volts, commonly used with subnanosecond ECL. The buried layers were not expected to carry signals, as in a conventional multilayer printed circuit board, since the interconnects were to be via wire wrap to special pins penetrating the logic panel.

A suitable method of bonding the leadless chip carriers to the universal logic panel was also required. Either of two choices appeared viable at the onset of the project: 1) direct solder bonding of the leadless chip carriers to the logic board, either by manual methods, wave solder, hot gas, or infrared methods, or by "vapor phase reflow" soldering; or 2) the use of connectors or sockets soldered to the universal logic panel in a fixed array, which would be capable of accepting a suitable leadless chip carrier. It was hoped that a combination of leadless chip carriers and suitably matched connectors for these leadless chip carriers would be feasible, thereby achieving maximum interchangeability and ease of component installation.

Because of the transmission line interconnects required for subnanosecond ECL, the use of high frequency terminator packs or buried layer resistor planes in the logic board was

considered. Because the intent of project is the development of components, boards, and technologies for rapid fabrication of high performance processors in a prototype, not a mass production, environment, the pack terminator approach demonstrates strong advantages over buried layer termination. Although a buried resistor terminator plane may exhibit slightly higher electrical performance than terminator packs placed on the component side of the board, the operation of terminator packs at high frequencies was demonstrated successfully in our previous work. Pack terminators allow the optimum transmission line protocol to be selected for the application at hand, whereas a buried resistor plane requires absolute prior knowledge of the exact locations at which the individual buried resistors are to be connected. It appeared possible to design high frequency terminator packs of even higher performance than those reported in Year 1 which would not degrade the electrical performance of the ECL dice, while maintaining the ability to select optimum transmission line protocols for each circuit string. The penalty for this electrical performance optimization is a small sacrifice in component packing density on the logic board.

Lastly, it would be necessary to identify suitable test equipment to verify the high frequency performance of the chip carriers, terminators, and logic board designs to be undertaken in the Year 2 effort.

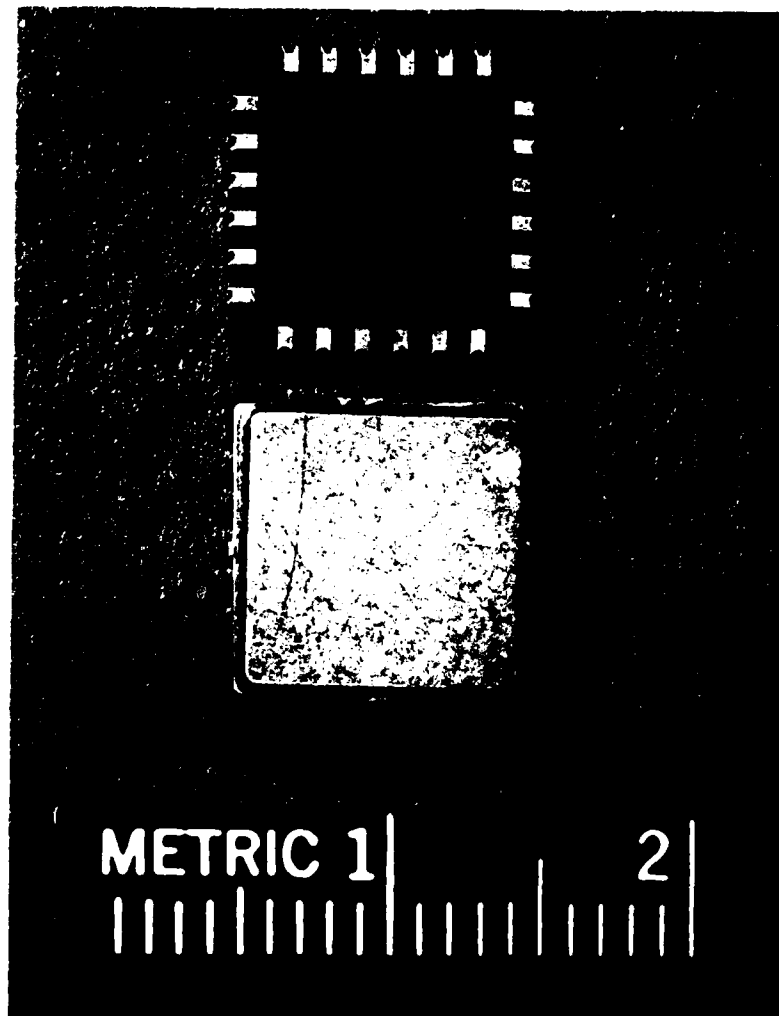
### SECTION III

#### SECOND LEVEL VERIFICATION OF ENHANCED ELECTRICAL PERFORMANCE FROM LEADLESS CHIP CARRIER/WIRE WRAP LOGIC PANEL COMBINATION

Before proceeding with the development of a fabrication technology based upon leadless ceramic chip carriers, it was necessary to verify previous estimates that such a combination would in fact demonstrate enhanced performance. The various steps followed in these verifications will be presented somewhat out of their sequential order of occurrence in order to clarify the intent of the study. In addition, an explanation of several of these steps will be deferred until later sections of the report for a similar reason.

Two similar but nonidentical styles of commercially available 24-pad ceramic leadless chip carriers were purchased from 3M Corporation and from Kyoto Ceramics Corporation (Kyocera). Figure 9 depicts both sides of the leadless chip carrier acquired from Kyocera. Note that the Kovar lid completely covers the cavity side of the leadless chip carrier. Arrangements were then made with Fairchild Camera and Instrument Corporation to use the 3M and Kyocera 24-pin carriers as the encapsulation for two part types from the subnanosecond ECL family of components, a multiple Or/Nor gate (F100102) and a 6-bit D-type register (F100151); these two part types had the highest speed ratings of any of the components then available from Fairchild. A

total of 200 leadless chip carriers were packaged in this manner, 100 of the 3M Corporation parts and 100 of the Kyocera



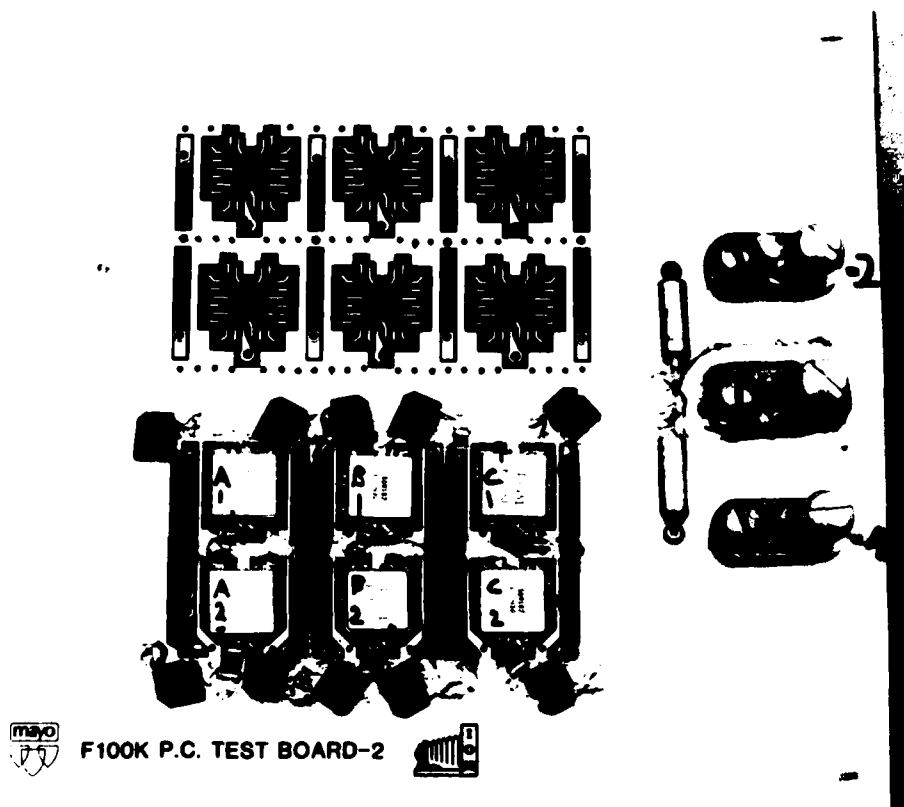
FRONT AND BACK VIEWS OF  
COMMERCIAL 24-PAD LEADLESS CERAMIC CHIP CARRIER  
MANUFACTURED BY KYOTO CERAMICS

Figure 9

parts; within each of these two groups, 50 parts were packaged with the register and 50 parts were packaged with the Or/Nor gates.

A small logic board was then fabricated with 12 patterns matching the footprint of the commercial leadless chip carriers. Figure 10 depicts the component side of this three-layer logic board (a ground plane layer on the component side, a buried -2 volt layer, and a -4.5 volt layer on the wire wrap side). Modified leadless wire wrap pins of a new style which were candidates for use in a full board design were then installed into the prototype three-layer board. There was a concern that earlier tests with leadless chip carriers (see Pages 92-97 of the Year 1 Interim Report) might have given overly optimistic results because wire wrap pins were not employed in the earlier experiment; twisted pair wires were merely soldered to the lead foils of the leadless chip carriers. The wire wrap side of this test vehicle is depicted in Figure 11; the lower pattern of six integrated circuits shows a circuit interconnected with single wire wraps; not shown are two later versions of this same board in which all interconnects were performed either with twisted pair wires or with wire wrappable coax. The top six circuit patterns in Figure 11 show the emplacement of eight of the wire wrap pins through etched and drilled holes which penetrate all three layers of the test board. Figure 12 depicts an expanded view of two of the logic components (a 6-bit register in the left

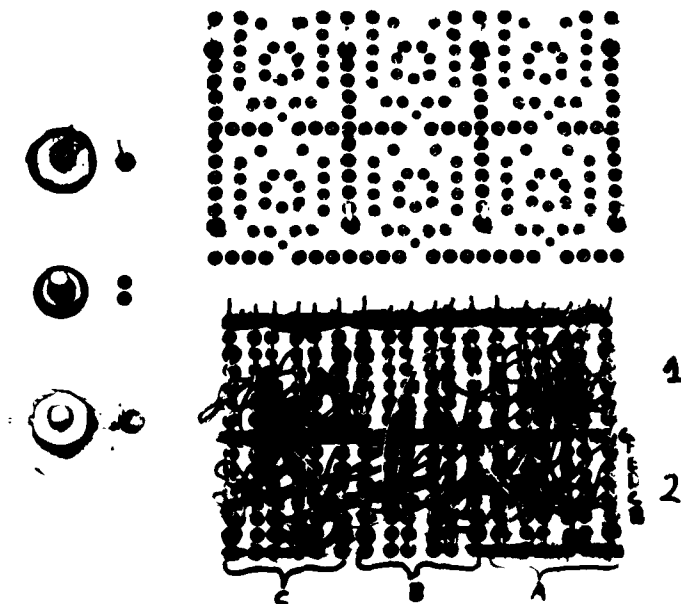
position and a set of Or/Nor gates in the right position), with a pair of terminator packs spaced horizontally along the bottom of the photograph. The square black structures are the 3.3 microfarad tantalum electrolytic capacitors used in the dual in-line package board (see Year 1 Interim Report) to bypass the -2 volt plane; the smaller gray structures placed at a 45° angle close to the chip carriers are NPO chip capacitors which decouple the -4.5 volt power plane to the ground plane. A small test circuit (see Year 1 Interim Report,



THREE-LAYER BRASSBOARD USED TO VERIFY  
HIGH FREQUENCY OPERATION WITH WIRE WRAP INTERCONNECTS

Figure 10

Figure 27, Page 72) composed of a data generator and several sets of registers in two ranks was fabricated on the logic board. First, all interconnects were performed with single wires, an interconnect scheme which is actually a violation of the protocols established in the Year 1 studies. The single wire tests were done for purposes of comparison with the second set of tests, in which all interconnects were via twisted pair wires, with one of the wires in the pair carrying

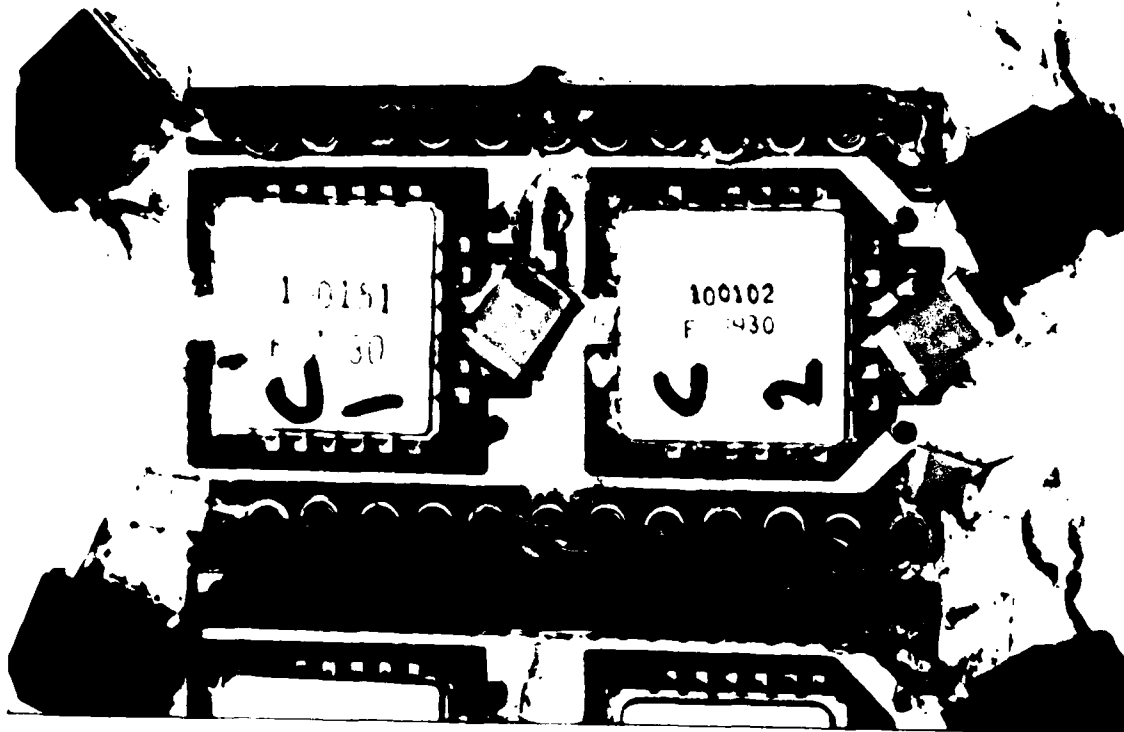


WIRE WRAP SIDE OF  
THREE-LAYER BRASSBOARD USED TO VERIFY  
HIGH FREQUENCY OPERATION WITH WIRE WRAP INTERCONNECTS

Figure 11

the signal and the other grounded at both of its ends. In the third test, all interconnects were performed with 75 ohm wire wrappable coax.

The results of these three sets of tests are depicted in Figures 13, 14, and 15. Figure 13 depicts test results from



CLOSEUP VIEW OF TWO LEADLESS CHIP CARRIERS ON PROTOTYPE  
BRASSBOARD CIRCUIT; LEFTMOST CARRIER CONTAINS  
AN ECL 6-BIT REGISTER; RIGHTMOST CARRIER  
CONTAINS FIVE ECL OR-GATES

Figure 12

the circuit fabricated with single wire interconnects. The upper panels of this figure depict the best case logic transitions from the circuit, measured from signal strings containing one source and one destination; the transitions are clearly subnanosecond. The lower panels depict an output bit from a data register operating at two clock rates; the 430 MHz clock rate was the highest frequency at which this circuit would operate. Data was then also recorded with the clock frequency set to a lower rate to allow an evaluation

PERFORMANCE OF PROTOTYPE SUBNANOSECOND  
ECL CIRCUIT EMPLOYING  
LEADLESS CERAMIC CHIP CARRIERS  
AND WIRE WRAP INTERCONNECT  
(Single Wire Connections; 25°C Forced Air Cooling;  
Soldered Copper Heat Studs;  
LCCs Soldered Cavity-Up to PC Board)

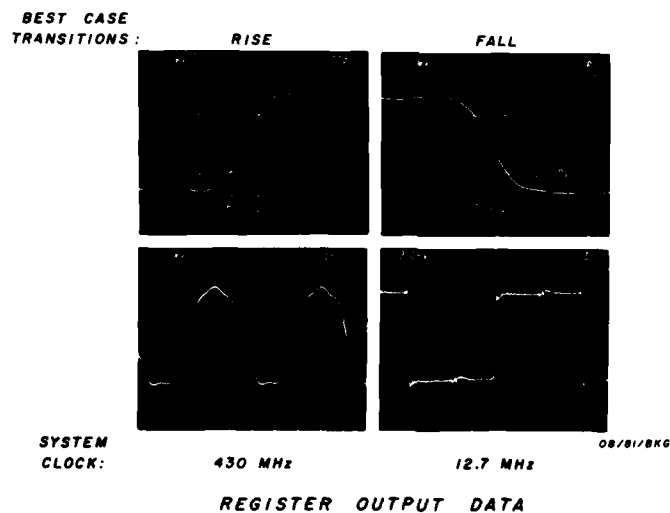


Figure 13

of the noise level on a typical signal. Except for the small noise spikes detected in the middle of the logic HIGH and logic LOW portion of the waveform, corresponding to the state changes of the clock drive gates (which transition at twice the rate of the data waveform depicted here), the signal is noise-free. Further measurements were not made on this circuit, as the wiring approach used in its construction is a violation of the design rules for subnanosecond ECL.

Figure 14 depicts data recorded from the same circuit but rewired with all interconnects via twisted pairs. The maximum

*PERFORMANCE OF PROTOTYPE SUBNANOSECOND ECL CIRCUIT  
EMPLOYING LEADLESS CERAMIC CHIP CARRIERS  
AND WIRE WRAP INTERCONNECT*

*(Twisted Pair Connections; 25°C Forced Air Cooling; Soldered  
Copper Heat Studs; LCCs Soldered Cavity-Up to PC Board)*

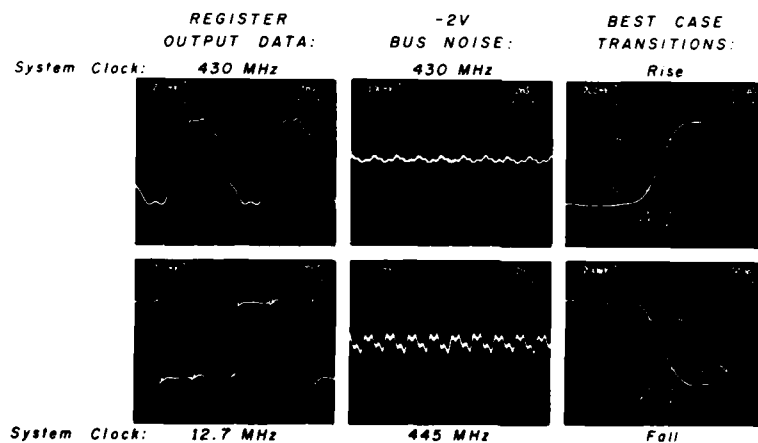


Figure 14

system clock rate was identical to that reported above for single wire interconnects. Data register waveform conformations at 430 MHz and at 12.7 MHz were also quite similar to those of the previous experiment. Note, however, that the noise on the -2 V bus was recorded at two frequencies, i.e., at 430 MHz, the maximum operating frequency of the circuit, and at 445 MHz, at which rate the peak-to-peak bus noise had increased to three times that at a frequency only 15 MHz less. Dependencies between system clock rate and bus noise have been observed before, and are thought to be caused by the electrical characteristics of the integrated circuits, board power

PERFORMANCE CHARACTERISTICS OF  
PROTOTYPE SYNCHRONOUS SUBNANOSECOND ECL CIRCUIT  
EMPLOYING LEADLESS CHIP CARRIERS  
AND WIRE WRAP INTERCONNECT

(498 MHz System Clock; Wire Wrappable  
Coax Interconnects; 25°C Forced Air Cooling;  
Soldered Copper Heat Studs; LCCs Vapor Soldered  
Cavity-Up to PC Board; Measurements at  $R_T$ )

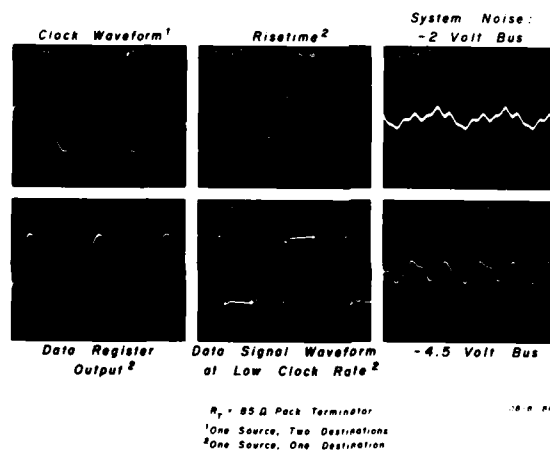


Figure 15

planes, and decoupling capacitors, which combine to form resonant circuits at specific frequencies. This problem has always been most noticeable in brassboard layouts, and less recognizable in finished logic panels with optimized ground and power planes.

Figure 15 depicts the results measured from the same circuit, but rewired with wire wrappable coax. This board demonstrated the best performance of the three, with the highest useable system clock rate observed to data for subnanosecond ECL (498 MHz), and the shortest risetimes and lowest levels of noise on the -2 volt and -4.5 volt power busses observed in this set of three experiments. It is not known at present whether this good performance was a random occurrence, or can be attributed to the wire wrappable coax interconnects. Though in all probability the former explanation is the correct one, additional testing will be performed on a full design multilayer logic panel optimized for leadless chip carriers to clarify this issue.

The single most important issue which appears to have been resolved by these three experiments is that significantly improved electrical performance can be attained by converting to leadless ceramic chip carriers and logic panels optimized for these new packages. On the basis of these tests, it was concluded that a full conversion to a packaging technology based upon leadless ceramic chip carriers would be worth the effort and would be undertaken.

# 1. Thermal Effects on Electrical Behavior With and Without Heat Sinks

Thermally induced effects on the electrical behavior of the components and logic board of Figure 10, observed during operational testing, was at variance with prior results at lower system clock rates. As will be explained in later sections of this report, it was necessary to mount the commercial ceramic leadless chip carriers on the circuit boards in a lid-up, dice-down configuration, i.e., with the ECL dice, and hence, the ceramic back layer of the leadless chip carrier, in direct contact with the epoxy circuit board (see Figure 12). The ECL components under test dissipated 500 milliwatts of power; since heat dissipation from the ceramic backs of the leadless chip carriers down into the solid epoxy board material is severely limited, and only a minimal amount of heat loss to the air-stream would occur, it appeared probable that thermally induced performance degradation or actual destruction of the ECL dice would occur.

These predictions were confirmed; the Kovar lids of the leadless chip carriers rapidly became uncomfortably hot without fan cooling; subsequent removal of the leadless chip carriers from the operating circuit board revealed charring of the board under the footprints of the leadless chip carriers. Irreversible chip failure occurred after 30 minutes of continuous operation if fan cooling of the board was not provided.

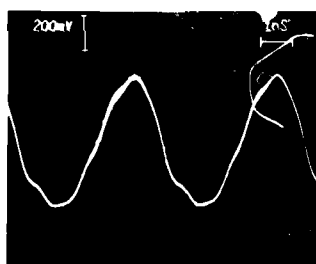
With approximately 500 lineal feet per minute (LFPM) air cooling, there was sufficient heat removal from the Kovar lids and the ceramic edges of the leadless chip carriers to preserve the integrity of the silicon dice.

To validate further the effects of thermal degradation of the electrical performance of the ECL dice, copper heat sinks were bonded to the Kovar lids of the leadless chip carriers with thermally conductive epoxy; electrical performance tests were then carried out with convection cooling into 25°C ambient air and with direct 500 LFPM fan cooling of the components. Heat sinks bonded to the Kovar lids do not provide an optimum thermal path for the leadless chip carriers, since the active thermal surface is the ceramic back of the chip carriers, which, as indicated in Figure 12, was in contact with the epoxy board and not exposed to the airstream. Figure 16 demonstrates the electrical performance of the operating circuit with the heat sinks positioned on the Kovar lids, and both with and without fan cooling of the logic board. The upper panel shows the circuit responding correctly to a 446.6 MHz system clock with fan cooling applied. The lower panel shows the electrical performance of the circuit at the same operating frequency, but two minutes after conversion from direct fan cooling to convective cooling. The performance of the ECL dice has degraded, since the circuit no longer tracks the 446.6 MHz system clock; it was necessary to decrease the frequency of the external clock by approximately 25 MHz before proper operation of the circuit was regained.

This electrical performance sensitivity to the thermal environment of the ECL dice, approximately -25 MHz, has not been observed in our prior studies, in all likelihood for the following reason. The subnanosecond ECL devices are temperature compensated (a combined worst case thermally induced voltage drift from all sources of -24 mV/°C) to assure electrical performance in a very narrow operating range, regardless of the ambient temperature of the dice, up to their time-

*EFFECT OF THERMAL ENVIRONMENT ON  
ELECTRICAL PERFORMANCE OF  
ECL D-TYPE REGISTERS  
ENCLOSED IN LEADLESS CHIP CARRIERS  
(446.57 MHz Clock; Copper Heat Studs  
Soldered to Kovar Lids;  
LCCs Mounted Cavity-Up on PC Board)*

*500 LFPM  
Forced  
Air Cooling  
at 25° C*



*Convection  
Cooling  
to 25° C  
Still Air*



Figure 16

temperature-product failure point. The dual in-line packages used in the Year 1 studies cannot operate at clock rates above 250 MHz, although the ECL dice are capable of 500 MHz performance; the resulting 2:1 speed performance margin in the prior tests prevented the thermal compensation networks from having to operate close to the maximum thermal and electrical limits of the ECL components simultaneously.

In the recent tests, however, the subnanosecond ECL dice were operated at 450 MHz and also at very high junction temperatures, i.e., at a point where the ECL gates and their thermal compensation networks are stressed to their thermal and electrical performance limits. As a result of the extremity of the operating regime, thermally induced changes in electrical performance are more apparent than at the lower frequencies employed with the dual in-line packages. Similarly, the large amount of metal in the DIP lead frames and the large surface area of the dual in-line packages are capable of sinking more of the thermal load from the dice than are the leadless chip carriers, particularly when the heat removal capacity of the 25 mil ceramic backing of the leadless chip carriers is defeated by improper installation. These tests demonstrated that the thermal design characteristics of candidate leadless ceramic chip carriers and the method used to attach them to a circuit board must be carefully considered for high power, high-speed digital devices.

## SECTION IV

### IDENTIFICATION OF LEADLESS CERAMIC CHIP CARRIERS SUITABLE FOR USE IN A HIGH POWER, HIGH FREQUENCY APPLICATION

#### 1. Review of Commercially Available Leadless Chip Carriers

At the onset of this project, we were aware that a wide range of leadless ceramic chip carriers were available from several vendors, including Kyoto Ceramics (Kyocera), Ceramic Systems, Inc., Augat, Inc., and 3M Corporation. As a result, it appeared virtually certain that a commercial leadless ceramic chip carrier could be identified with physical characteristics suitable for use in this project; in the research plan presented to Air Force Avionics Laboratory/AADE-3 in November 1979, the Statement of Work proposed the identification of a suitable leadless chip carrier by a review of the commercially available part types.

However, a review of the physical designs of the commercially available leadless chip carriers, and the results of the electrical and thermal studies reported in the previous section, indicated that the presently available leadless chip carriers are unsuitable for high power, high-speed silicon ECL or CML components. First, as will be described below, the commercial leadless chip carriers are designed to be mounted on a circuit board with their ceramic surfaces (i.e., the surface

opposite the die cavity) in direct contact with the printed circuit board (see Figure 12). As a result, air cooling of the commercially available chip carriers is infeasible, since optimum cooling could only be assured by placing the leadless chip carrier "cavity down" ("Kovar lid down"), "ceramic face up" on the printed circuit board. In the "lid-down" configuration, the ECL dice is separated from the airstream, only by the 20 mil thickness of the ceramic face layer of the leadless chip carrier ("Layer 1" in Figure 26).

However, in the "lid-up" mounting mode, the thermal paths are down into the printed circuit card, or laterally through the ceramic back of the leadless chip carrier, then up through its sides and into the Kovar lid; the latter is clearly a longer and higher impedance thermal path. Satisfactory cooling may be achieved with these commercial leadless chip carriers if the printed circuit board contains a cold plate or a honeycomb through which liquid Freon is pumped, an approach which has been taken by several manufacturers. However, these printed circuit boards are expensive and the design cycles for these boards are relatively long, as confirmed by the Information Systems Group of Control Data Corporation. Since this project is attempting to develop techniques for rapid fabrication and turnaround of ultra high-speed systems, the long lead times required for internally cooled honeycomb boards are unacceptable. Airstream cooling was considered mandatory for ceramic leadless chip carriers suitable for a rapid turnaround prototyping environment.

The commercially available leadless chip carriers cannot be inverted for direct forced air cooling by a moving airstream because of several fundamental design features. Figure 17 is an edge-view photomicrograph of a conventional 24-pin leadless chip carrier positioned in the "ceramic surface up", "Kovar lid down" configuration. The normal electrical contact paths between the die cavity and the outer boundaries of these leadless chip carriers are tungsten leads which traverse the body of the leadless ceramic chip carrier from the die attach area to the small vertical edge castellations which appear as light vertical columns in this figure. The black mass in the lower half of the figure represents the printed circuit card viewed in cross section, which is in direct contact with the 10 mil thick Kovar lid of the leadless chip carrier. The castellations must make electrical contact with metal traces on the upper surface of the printed circuit board; clearly, however, the Kovar lid creates a physical gap between the castellations and the circuit board which is too large to be bridged by a solder ball.



CONVENTIONAL LEADLESS CHIP CARRIER PLACED  
LID DOWN ON SIMULATED LOGIC BOARD SURFACE.  
NOTE GAP BETWEEN CASTELLATIONS AND "BOARD".

Figure 17

Figure 17 also shows that each castellation is itself composed of two areas: the upper portion, appearing as a light gray vertical column, is the actual gold plated electrical conduction path. At the bottom of each castellation is a region which is deliberately not gold plated, thereby serving as a guard band to prevent short circuits between the plated portion of each castellation and the Kovar lid. Note that the upper portion of each castellation is plated up to the ceramic surface of the leadless chip carrier; though not visible in this photograph, the metallization extends onto the back ceramic surface of the carrier as well. This structure can be more fully appreciated in Figure 18, which is a higher magnification photomicrograph of the edge of the same leadless chip carrier. The castellation structures are comprised of a plated upper region and an unplated guard band adjacent to the Kovar lid; the gold plated portion of the castellation extends onto the ceramic back of the leadless chip carrier. Hence, direct electrical contact between the plated portion of a castellation and a trace on the circuit board in the lid-down configuration is impossible.

The unplated guard band in the castellation is a generic feature of all commercially available leadless chip carriers designed for cavity-up mounting; Figure 19 depicts an edge view of an experimental 100-pad ceramic leadless ceramic chip carrier also intended for cavity-up mounting. This chip carrier was photographed without a Kovar lid; each castellation



PHOTOMICROGRAPH OF EDGE CASTELLATIONS  
IN CONVENTIONAL LEADLESS CHIP CARRIER

Figure 18

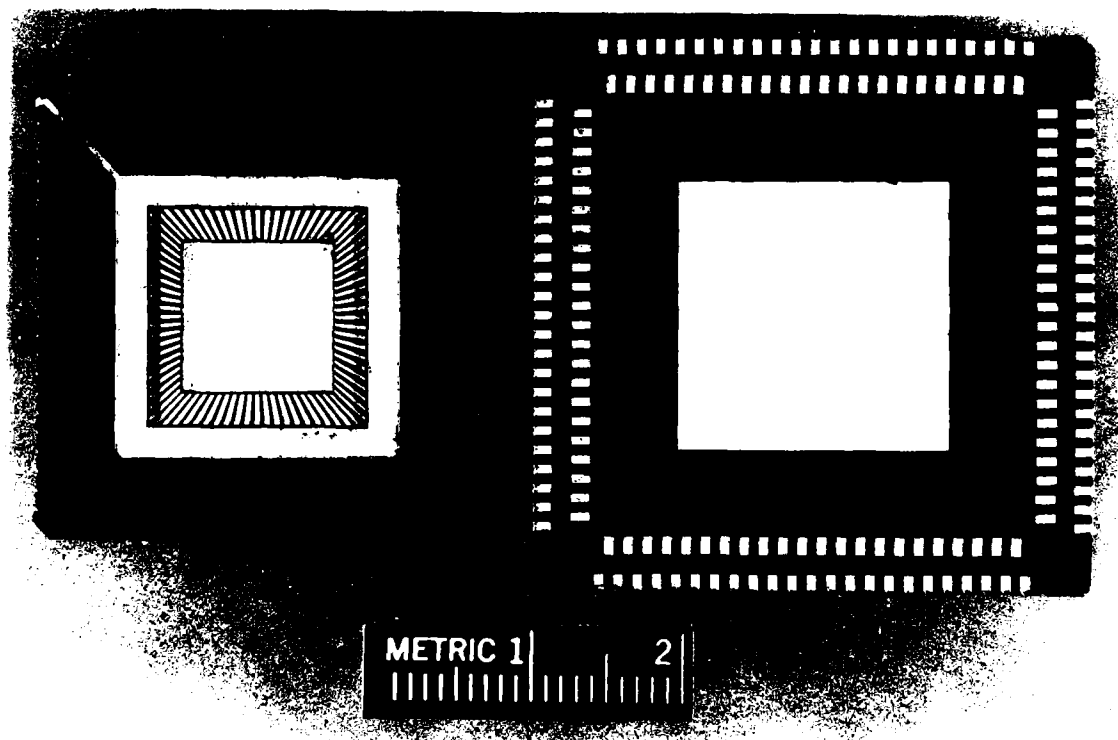


EDGE VIEW OF AN EXPERIMENTAL  
100-PAD LEADLESS CERAMIC CHIP CARRIER

Figure 19

is again composed of a plated and an unplated region; in this photo, the cavity side of the chip is positioned face down against the black support structure. Figure 20 depicts surface views of experimental 80 and 100 pad leadless chip carriers, showing that their construction is somewhat different from the smaller carriers.

Figure 21 shows an edge view of a 68-pad JEDEC Leadless Type A ceramic chip carrier, specifically designed to be

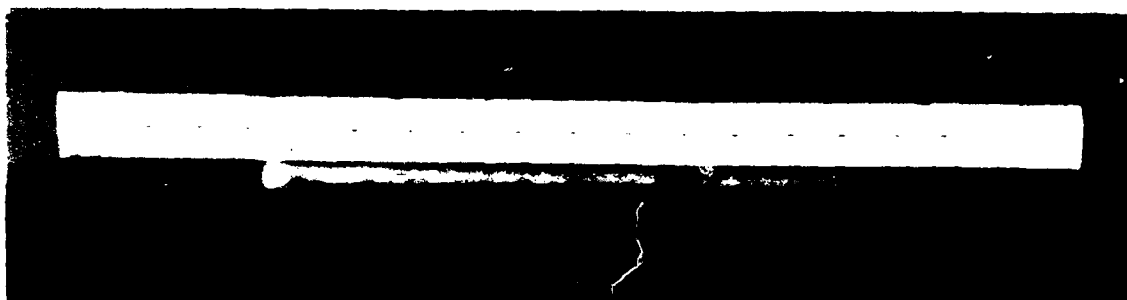


TWO EXPERIMENTAL LEADLESS CERAMIC CHIP CARRIERS.

LEFT: 80-PAD CARRIER.

RIGHT: 180-PAD CARRIER WITH TWO ROWS OF CONTACTS.

Figure 20

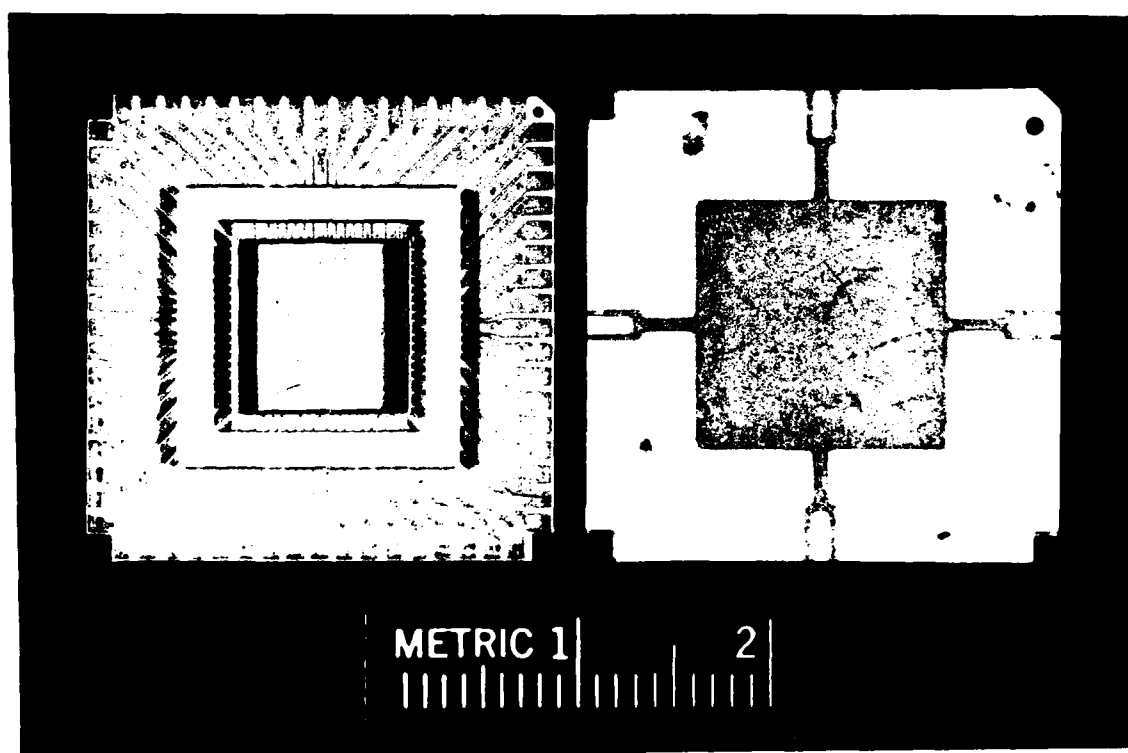


EDGE VIEW OF LEADLESS TYPE A 68-PAD  
LEADLESS CERAMIC CHIP CARRIER. NOTE "ELECTROPLATING

Figure 21

mounted in a leadless chip carrier connector (socket) with electrical contacts on the lower surface (the cavity side) of the leadless chip carrier. The lid seal ring is on the innermost portion of the chip carrier (see Figure 22). This structure is free of edge castellations, and is designed for mounting with the ceramic back facing the airstream; nonetheless, direct contact with the printed circuit board cannot be made because of the spacing effect of the raised seal ring for the Kovar lid. Figure 22 shows that the contact pads on the cavity side of the leadless chip carrier are designed to be contacted only by the pins of a ceramic chip carrier connector. The ceramic back surface of this component includes a gold plated heat spreader and attachment point for copper heat studs. This package, though addressing several of the issues raised in the discussion of the 24-pin leadless chip carriers, nonetheless possesses many of the same limitations described above for the small commercial leadless chip carriers.

Lastly, the possibility was considered that suitable connectors could be identified for the commercially available leadless chip carriers which would circumvent the difficulty of solder bonding these chip carriers directly to a printed circuit card. However, several of the connectors investigated in this study (see later sections) contact the chip carriers by means of spring loaded wires which are positioned to lie within the grooves of the castellations themselves. Hence, the partial metallization and guard band approach used in many of



FRONT AND BACK VIEW OF JEDEC LEADLESS TYPE A  
LEADLESS CERAMIC CHIP CARRIER

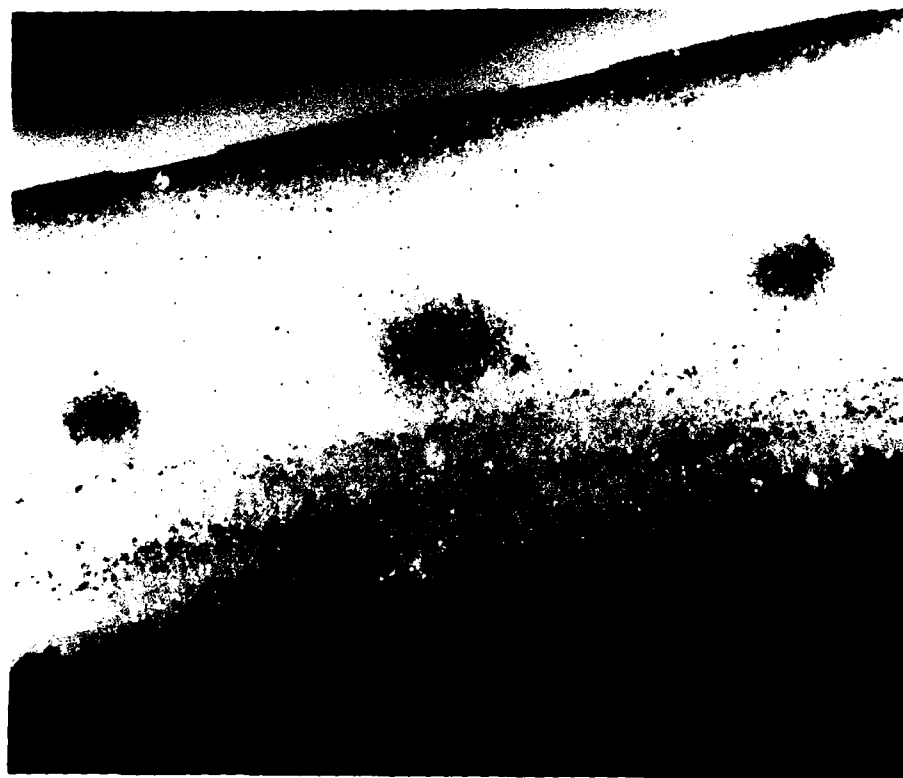
Figure 22

the commercial chip carrier designs appeared likely to cause uncertain electrical contact between the spring loaded wires of the connectors and the partially metallized regions of the castellations; in addition, short circuits between the contact wires in the connector and the Kovar lid seemed possible. To guarantee a good electrical contact between the spring loaded wires of chip carrier connectors and the chip carrier castellations, it appeared necessary to plate the entire length of each castellation, and to modify the Kovar lid attachment to minimize the possibility of short circuits between the connector contacts and the lid.

Another deficiency of the commercially available 24-pin leadless chip carriers for high frequency devices is an inadvertent negative impact of the manufacturing process on the electrical performance of the leadless chip carriers. Figure 21 reveals the presence of small uniformly spaced dark dots along the edge of the 68-pin ceramic leadless chip carrier, which are more apparent in Figure 23, a high resolution photomicrograph of this same chip carrier. The small dark segments along the upper edge of the chip carrier are cross section views of the metallization pads on the facing surface of the chip carrier; it is not coincidental that the small dark lines in the central body of the chip carrier are in approximate vertical alignment with the contact pads on the surface of the carrier. The dark lines buried within the carrier are cross sections through small metal fingers which extend into

the ceramic and form a Y-shaped connection to the signal lines in the body of the chip carrier. These "plating fingers" are the conduction paths for the flow of D.C. current required by the electroplating step in the manufacture of the leadless chip carriers; one of these thin metal lines is associated with each of the signal conductors.

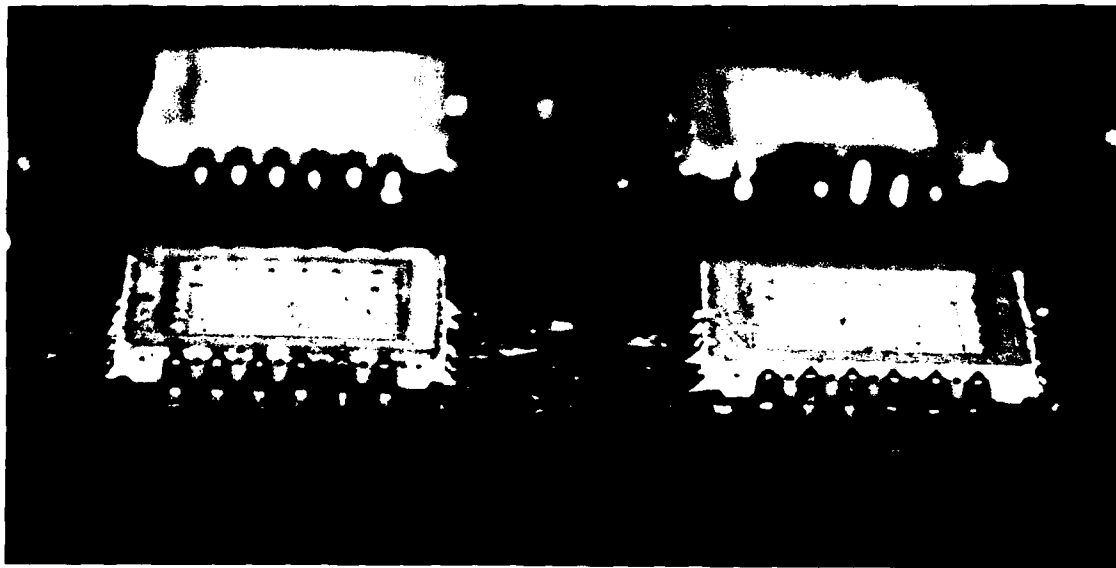
The electroplating fingers increase the parasitic shunt capacitance between adjacent signal lines and also between the



PHOTOMICROGRAPH OF 68-PAD LEADLESS TYPE A  
CERAMIC CHIP CARRIER SHOWING "ELECTROPLATING FINGERS".

Figure 23

signal lines and the AC ground planes within the chip carrier, i.e., the die attach plane in the center of the chip carrier and the heat spreader on the back surface of the carrier as well. Figure 24 depicts two of the 24-pin leadless chip carriers soldered to a test circuit board in the cavity-up configuration. Note the small dark dots along the edges of both chip carriers, which, as in the previous figure, are the electroplating fingers for the conductors in the signal layer. These small added capacitance effects, irrelevant for low frequency TTL devices, are nontrivial additions to the overall parasitic characteristics of the chip carrier when used in



CONVENTIONAL 24-PAD LEADLESS CHIP CARRIERS REFLOW SOLDERED TO CIRCUIT BOARD. NOTE DARK DOTS ALONG EDGES, WHICH ARE ELECTROPLATING FINGERS FOR SIGNAL CONDUCTORS AND DIE ATTACH AREA.

Figure 24

high frequency applications. Although upon first consideration it would appear possible for the manufacturer to use the conductors in the castellations for electroplating the depth of the castellations would complicate the plating; the electroplating tabs on the edges of the carrier are much more convenient from the viewpoint of the manufacturer.

The parasitic shunt capacitances created by the electroplating fingers is further compounded by the presence of yet another set of plating fingers, which may be detected in Figure 24 between the second and third from rightmost castellations in each of the chip carriers. A second dot slightly closer to the printed circuit board is an edge view of a plating finger which extends from the die attach metallization to the edge of the chip carrier. In all chip carriers manufactured by 3M Corporation, at least one and sometimes two plating fingers extend from the die attach area to each edge of the chip carrier. These fingers are used in the electroplating of gold onto the die attach surface, and in several designs pass directly under the signal traces in their journey to the edge of the chip carrier. These electroplating extensions traverse the chip on the lowest, or first, layer of the chip carrier, while the signal lines are carried on the second ceramic layer. The die attach plating fingers increase the shunt capacitance between the signal leads and ground for the second and third from rightmost contacts on each edge of the chip carrier; thus,

two out of the six signal leads on each edge of the chip carrier have electrical performance different than (worse than) that of the other leads along the same edge of the carrier. Although the die attach plating fingers would not be a problem for TTL and MOS components, they appeared to cause an unnecessary degradation of the electrical performance of the chip carrier merely to achieve a manufacturing convenience.

The above studies indicated that the best resolution of the thermal, mechanical, and electrical limitations identified in commercial leadless ceramic chip carriers would be by the design of a chip carrier optimized for the high power dissipation, high frequency operating characteristics of subnanosecond ECL dice; it would also then be possible to correct several mechanical deficiencies which had been identified in the commercial carriers. The initiation of a new design of a suitable leadless chip carrier was discussed with a staff member at AFWAL/AADE-3 (W.A.A.) and briefly with Dr. R. Vernon, chairman of the JEDEC JC-42 Standards Committee for leadless chip carriers; the decision was made to undertake a new design.

## 2. Design of New Leadless Ceramic Chip Carriers for Use in a High Power Dissipation, High Frequency Environment

When the design effort for the new leadless chip carrier was undertaken, we were not aware that the JEDEC JC-42 Standards

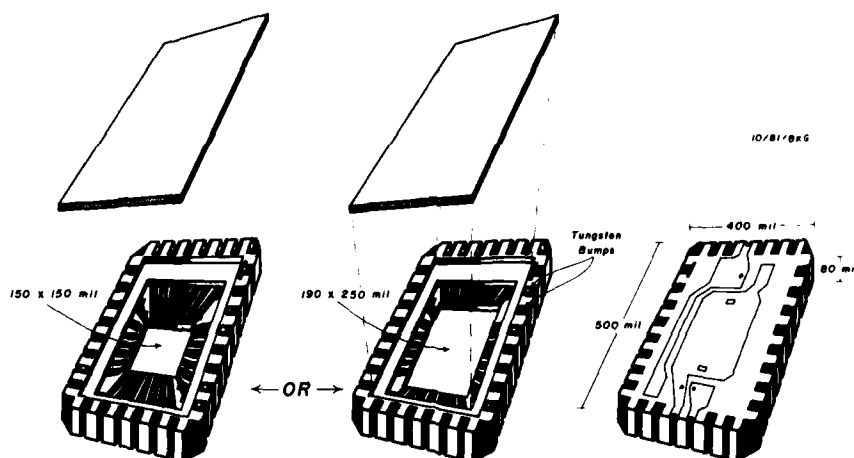
Committee was then preparing a preliminary leadless chip carrier guideline for lid-down mounting. This guideline came to our attention in the fall of 1980, after our own development was well under way; thereafter, we tried where possible to accommodate our design to the preliminary JEDEC standard (referred to as JEDEC Type D). Nonetheless, it soon became clear that many design details would have to disregard the proposed JEDEC Type D standard. A new leadless ceramic chip carrier for high frequency, high power applications would have to be suitable for mounting in the lid-down, ceramic surface up configuration, thereby guaranteeing maximum aircooling efficiency.

Between September 1980 and July 1981, three complete design iterations of a small leadless ceramic chip carrier were undertaken, leading to the design depicted in Figures 25 and 26. Figure 25 shows the cavity side and the back surface views of the leadless ceramic chip carrier currently undergoing fabrication. The thermally mandated design features of this chip carrier are apparent in these views. Provision has been made to employ a recessed lid by converting the chip carrier design from a three layer to a four layer structure. As depicted in Figure 26, the first layer carries the die attach surface; the second layer contains the signal pin leadouts and provides the attachment points along the edge of the die well for the wire bonds to the die (or, to reduce series inductance, the newer beam lead bonds). The third layer is a spacer layer (the new

layer added in this design) which provides a shelf for the lid seal ring onto which a small Kovar lid can be recess-mounted.

Lastly, the uppermost or fourth layer of the chip carrier supports a number of small tungsten bumps which are extensions

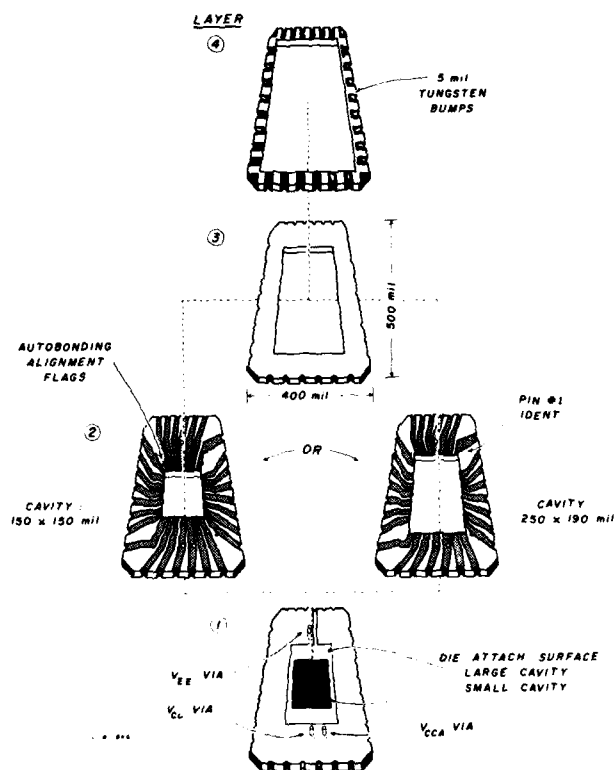
AIR-COOLED LEADLESS CERAMIC CHIP CARRIER FOR  
HIGH POWER, HIGH FREQUENCY DIGITAL INTEGRATED CIRCUITS  
(28 Pads; Two Die Cavity Versions; Recessed Lid  
For Mounting Die Well Down; 94% Alumina Substrate)



FRONT AND REAR VIEW ARTISTS CONCEPTION OF NEW  
MAYO-DESIGNED LEADLESS CERAMIC CHIP CARRIER

Figure 25

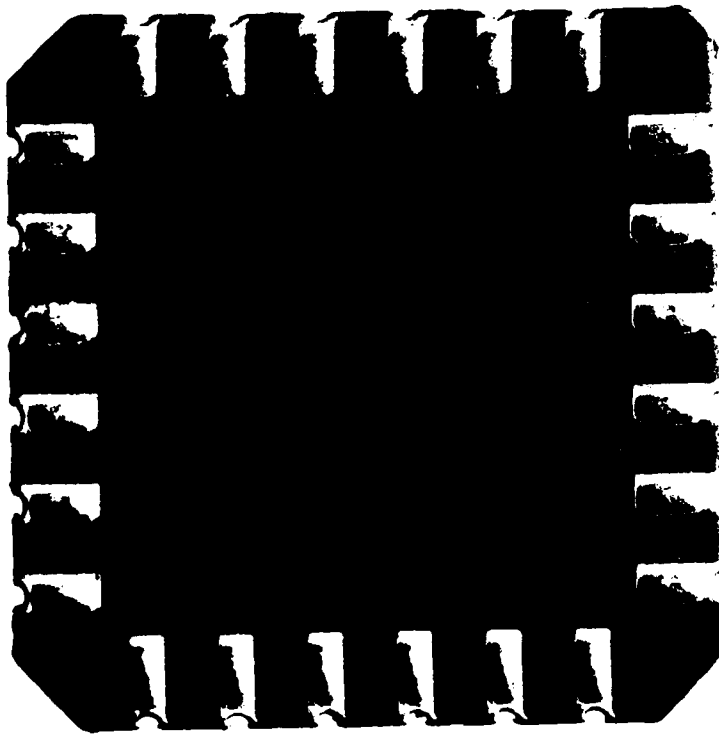
AIR-COOLED LEADLESS CERAMIC CHIP CARRIER  
 FOR HIGH POWER, HIGH FREQUENCY  
 DIGITAL INTEGRATED CIRCUITS  
 ( 28 Pads, Two Die Cavity Versions ;  
 Recessed Lid for Mounting Die Well Down ;  
 94% Alumina Substrate )



EXPLODED VIEW OF MAYO DESIGNED  
 LEADLESS CERAMIC CHIP CARRIER

Figure 26

of the signal traces on the second layer of the chip carrier. The artist's conception of Figure 25 illustrates these tungsten bumps, which are more apparent in the photomicrograph of Figure 27. This test blank was fabricated by Kyoto Ceramics Corporation to demonstrate the ability to fabricate these structures, which are 5 mils high, 30 mils long, and approximately 20 mils wide. The tungsten bumps serve two functions



LEADLESS CERAMIC CHIP CARRIER TEST BLANK  
FABRICATED WITH 5-MIL HIGH  
TUNGSTEN CONTACT BUMPS

Figure 27

in the Mayo-designed chip carrier. First, manufacturing tolerances could create a situation in which the Kovar lid is not recessed adequately and might protrude 1-2 mils above the surface of the chip carrier. The 5 mil tungsten bumps will allow the chip carrier to be surface mounted in the lid-down configuration whether or not a perfect recessed lid arrangement is achieved in every chip carrier. Second, these bumps will serve either as solder attach points or as contact points for a chip carrier connector. When solder attachment is employed, the concentration of heat by the tungsten bumps is expected to provide improved high quality solder reflow connections.

Although the chip carrier of Figures 25 and 26 is designed for inverted mounting, provisions have also been made for lid-up mounting; note that the edge castellations extend from one surface of the chip carrier to the other and can be plated along their entire length, since there will be no possibility of short circuits to the Kovar lid. The chip carrier can thus be solder mounted to the printed circuit board lid-up using fillet solder joints, or may be mounted lid-up or lid-down in a chip carrier connector. In the lid-up mounting configuration, testing of the chip carrier from the component side of the board will be straightforward since the tungsten bumps serve as contacts for handheld probes.

Figure 25 depicts the ceramic back surface of the chip carrier on which will be plated a metal heat spreader, which

is the solder attachment point for a copper heat stud. The two small flag-shaped structures, which improve the electrical characteristics of the chip carrier, will be described in succeeding paragraphs. To improve further the dissipation of heat through the back of the chip carrier, this Layer 1 was made as thin as possible. Although the original design specified a 20 mil thickness for Layer 1, this dimension had to be increased to 25 mils to assure sufficient mechanical strength.

Finally, to improve thermal performance, 96% powdered beryllia was considered as the fundamental substrate material for the leadless chip carrier, since the thermal conductivity of beryllia is 6.44 times that of alumina (.38 versus .059 (cal/sec)(cm<sup>2</sup>(°C/cm))). However, at the onset of this project, a vendor could not be identified either in the United States or in Japan willing to manufacture components with this material, since beryllia powder is extremely toxic (causing pulmonary berylliosis); its use is legally prohibited in Japan. Recently, a vendor of ceramic structures capable of manufacturing beryllia leadless chip carriers in a sealed environment has been identified; it is now planned to refabricate the chip carrier of Figures 25 and 26 in beryllia later in this research study. The first set of chip carriers will be fabricated with 94% alumina, since many of the design features of the new carriers are independent of the fabrication material.

The design features included to improve the electrical performance of the Mayo-designed leadless ceramic chip carrier may also be observed in Figure 26. The rightmost panel of Figure 26 depicts the back surface of the chip carrier, including the square gold heat spreader and attachment point for a soldered heat stud. Note that the metallization is extended to the corners of the chip carrier, which are beveled at a 45° angle and are metallized and castellated for solder connection to ground plane contacts on the printed circuit board; a tungsten bump is also positioned at each of the four corners for the same purpose. Connection of the back metallization and the soldered heat stud to ground allows these structures to serve as an electrical shield for the ECL dice, and also to provide a decoupling capacitance of approximately 100 pF between die attach metallization (which is connected to the -4.5 volt bus) and ground. At the high frequencies of subnanosecond ECL, a 100 pF capacitance provides a nontrivial decoupling effect to minimize  $V_{EE}$  voltage transients observed by the ECL die.

Conversely, the back surface metallization may increase the parasitic input shunt capacitance of the signal leads; this increased shunt capacitance has been calculated to be less than .1 pF, an acceptable level if correct. These estimates will be verified by direct measurement at 1 GHz on the leadless chip carriers fabricated with and without the back metallization (see the description of a new high frequency

impedance measurement technique in a later section of this report). Hence, the composite effect of the heat spreader metallization is still unproven; if the electrical performance of the signal leads is degraded sufficiently by the back surface metallization, it will be deleted from the chip carriers manufactured thereafter.

The back surface of the chip carrier also supports two small rectangular metallized areas electrically connected to a center castellation on two edges of the chip carrier; these two castellations are the -4.5 volt supply pads for the chip carrier. Figure 26, an exploded view of all four layers of the chip carrier, displays small solid vias connecting these rectangular metallization areas to the internal -4.5 volt bus leads on Layer 2. The ground runs from the corners of the chip carrier and the metallized rectangular patches are to be attachments for small 4700 pF NPO chip capacitors, which can be soldered on the back of the chip carriers to further decouple the -4.5 volt die attach plane to ground.

Figure 26, an exploded view of all four layers of the Mayo-designed leadless chip carrier, indicates two additional features intended to improve the electrical performance of the chip carriers. First, no electroplating fingers between the signal lines are evident on Layer 2; Kyoto Ceramics believes that they can manufacture these chip carriers and achieve a high electroplating quality without the plating fingers. Note

also that the gold plated die attach area on Layer 1 of the chip carrier supports only a single electroplating finger 10 mils in width extending to the edge of the chip carrier. Although an attempt was made to eliminate even this finger, the alternate approach to the electroplating of the die attach area would have caused a small portion of this region to remain unplated, thereby preventing large chips from being implanted in the die cavity by the normal eutectic scrub technique used in the die attachment process. The remaining electroplating finger will increase the parasitic shunt capacitance of the two signal leads closest to this finger. This slight degradation for only a single lead may have to be tolerated.

The chip carrier currently in fabrication is rectangular in shape, with external dimensions 450 x 550 mils, supporting 32 contact pads, with 7 contacts on each of the two short edges and 9 contacts on each of the two long edges (Figure 25). The rectangular configuration resulted from a series of performance tradeoffs constrained by a design parameter of subnanosecond ECL which is quite different from those of low-speed TTL and MOS integrated circuits. Maximum performance of subnanosecond ECL dice cannot be mirrored by higher system performance unless each circuit board can be laid out with arithmetic, logic, and memory functions juxtaposed to other components with which they must communicate. Grouping of components by function, i.e., all memory components together, all arithmetic components together,

etc., can extract a severe performance penalty due to extended propagation delays between communicating but widely separated parts equivalent to the performance improvement gained in the dice themselves. If functions are to be placed on a board where needed, the layout task becomes very difficult if a multiplicity of chip carrier size is required. This problem appeared in the design of the logic board described in the Year 1 Interim Report (see Year 1 Interim Report, Pages 27-29).

As a result of these lessons learned during the Year 1 research, a strenuous attempt was made to minimize the total number of package types and package footprints, thereby allowing optimization of the layout of universal boards or of special-purpose multilayer printed circuit cards. Minimization of the number of different package sizes is also of benefit for computer-aided design programs, since a proliferation of package sizes and shapes adds to the complexity of the layout, component placement, wire routing, and optimization subroutines. Three chip carrier package sizes were selected tentatively for the Mayo work, the first of approximately 28-pin, 450 mil square size, the second reflecting the JEDEC Type A 68-pad leadless ceramic chip carrier standard, and a third package in the pin size range of 140-200 pins (Figure 20).

The first goal of the project was a design for the smallest of these three leadless chip carriers. A review was performed

of the range of die sizes for devices already extant in the subnanosecond ECL family, currently under development, or planned for this same family, including logic, arithmetic, and memory parts, which would require 32 or fewer contacts. Our first attempt was with a 28-pin square leadless chip carrier of outer dimensions 450 x 450 mils, with a maximum die attach area of 185 x 185 mils. Note that for a given die well area, a leadless chip carrier employing a recessed lid for lid-down mounting must always be larger than the equivalent chip carrier using a surface mounted Kovar lid, since the recessed lid requires a mounting recess and lid seal ring which increases the size of the chip carrier by approximately 100 mils in each coordinate. The 28-pin leadless chip carrier designed for recessed lid mounting yielded a die attach area which appeared too small to the Mayo group, an opinion which was strongly corroborated by the memory design staff at Fairchild. Although it was clear that all arithmetic and logic parts requiring fewer than 32 padouts would easily fit into the die well size of a square 28-pin recessed lid chip carrier, J. Steinhelfer of Fairchild pointed out that even the current F100470 4K x 1 memory component would barely fit into such a package.

The internal dimensions of the chip carrier were then increased by an additional 50 mils in both dimensions, to 500 x 500 mils, resulting in a die attach area of 235 x 235 mils and containing 32 padouts. Although an increase in the number

of padouts above 24 was not itself a design goal, nonetheless it appeared reasonable to provide the extra padouts for future expansion requirements since their inclusion would not affect the cost of the chip carriers and would not degrade their electrical performance. The die well size of this 32-pad chip carrier was compared with all existing and planned memory parts, and it soon became obvious that the 25 nsec 16K x 1 ECL static RAM memory parts currently in early test phases at Fairchild (the F100480) could be placed in these carriers only with difficulty, and not at all for the early versions, which are 30% larger than the planned size of the production chips.

Discussions between the Fairchild engineers and the Mayo group revealed that the memory components all display a rectangular aspect ratio; the memory cells are square, but the auxiliary decoding logic positioned along the periphery of the memory array result in a rectangular footprint. It became apparent that the optimum solution to a single chip carrier footprint for all memory, logic, and arithmetic parts, either presently available or planned, was the design of a rectangular chip carrier of external dimensions 450 x 550 mils, carrying 32 pads and with a maximum internal die well dimension of 215 x 300 mils. A single die well and chip carrier footprint could then incorporate parts from a few thousand mil<sup>2</sup> area, such as the F100102 five section OR-gate, to the largest memory parts now planned, 64K x 1 and 16K x 4 memory components of greater than 30,000 mil<sup>2</sup> area.

The manufacturing engineering staff at Fairchild pointed out that the wire bonds between the edge pads on the ECL dice and the bonding attachment points on the leadless chip carrier must be within a critical range of lengths, i.e., not less than 30 mils nor greater than 100 mils. If only a single cavity size were used, the length of the bonding wires required for the smallest ECL dice would be too great to survive shock and vibration tests. To alleviate this problem while maintaining the capability for maximum die size in this footprint, Figure 26 shows that Layer 2, which creates the boundary of the die well cavity and supports the bond wire attachment points of the chip carrier, will be manufactured in two versions, one of which will accommodate small ECL dice of a few thousand mil<sup>2</sup> area, and a second pattern which defines a larger die well cavity and will accommodate the components of larger than 30,000 mil<sup>2</sup> area. Since the other three layers of the chip carrier are unaffected by the alternate versions of the second layer, the additional cost to manufacture two alternate versions of Layer 2 is acceptable.

Although there may be a slight degradation in electrical performance for the smallest die sizes due to the extra required lengths of signal leads on Layer 2 of the chip carrier, this additional length is only 50 mils worst case for any lead, which will add approximately .5 nanohenries of series inductance and a fraction of a picofarad of shunt capacitance; the propagation delay increments will be on the order of 2.5 psec. These minor

performance degradations may be tolerated to achieve standardization on a single leadless chip carrier accepting a wide variety of part types. Fairchild and Mayo engineers have identified feasible bondout patterns for all presently available or currently envisioned memory, logic, and arithmetic parts if encapsulated in this new leadless chip carrier.

Also incorporated in the design of this package are several advantageous mechanical features. The tungsten bumps may to some extent dissipate the stresses on the chip carrier which would occur if the chip carriers were flush mounted and fillet soldered at their castellations to the printed circuit cards. In addition, the tungsten bumps will elevate the chip carrier above the surface of the board by 4-6 mils, as depicted in Figure 28, thereby allowing flux solvents to remove the mildly activated fluxes from the interstices between the chip carrier and the circuit board. Complete flux removal should



EDGE VIEW OF LEADLESS CERAMIC CHIP CARRIER  
TEST BLANK SHOWING SPACING EFFECT  
OF 5 MIL TUNGSTEN BUMPS

Figure 28

reduce corrosion of the Kovar lid and the surface conductors on the logic board. Figures 25 and 26 show four triangular patterns in the interior corners of the second layer of the chip carrier. These triangular structures were included in the design to allow modern optically registered autobonders to accept this package, since the optical sensing units of the autobonders can align on the triangular shapes for bonding purposes. Hence, this package can be used immediately for manual bonding, and will not require a redesign when autobonding becomes widely used.

It was necessary to assure that the evolving Mayo leadless chip carrier design would include only those features compatible with conventional eutectic scrub die installation, wire bonding, and lid sealing operations, but would also accommodate planned improvements in manufacturing techniques such as autobonding and beam lead bonding. The Mayo group initiated the design of the early chip carriers, and then enlisted the assistance of the packaging group of Fairchild and Camera Instrument Corporation, and an engineer from Kyoto Ceramics Corporation. This collaboration has resulted in a package which is manufacturable, which appears to be well suited to the growing requirement for an air-cooled high-power leadless ceramic chip carrier for subnanosecond ECL dice, and which is optimized for the Mayo requirement of a single footprint leadless chip carrier usable in a system prototyping environment. In addition, the chip carrier can be attached

to a logic panel either lid-down, with electrical contact by means of the tungsten bump and solder fillet joints to the edge castellations, or without the back metallization for lid-up mounting via fillet solder joints to the castellations only. Further, the complete metallization of the castellations along their entire length makes these devices adaptable to use with chip carrier connectors as well, since the chip carrier connectors can make electrical contact with the castellations throughout their entire length.

Tooling charges were assessed for this package for both a soft tooling approach, which would allow the fabrication of only 2,000 pieces, or hard tooling, at twice the expense but with unlimited production feasible. Since Fairchild Camera and Instrument Corporation plans to use this leadless chip carrier as their standard small air-cooled, high-power, high frequency chip carrier package, and since the Mayo Research Group will need the empty leadless chip carriers for other unrelated projects, large production runs are envisioned. As a result, hard tooling will be undertaken from the outset.

## SECTION V

### DESIGN AND DEVELOPMENT OF MULTILAYER WIRE WRAP UNIVERSAL LOGIC PANEL OPTIMIZED FOR LEADLESS CERAMIC CHIP CARRIERS

In parallel with the development of the leadless ceramic chip carrier described in the previous section, design was initiated of a suitable multilayer universal logic panel which would support a wire wrap interconnect technique. The logic panel, currently in final layout, appears in artist's conception in Figure 29. Every design feature of this board has undergone numerous refinements, as will be indicated below. The board will be described in its present form, with a general explanation of each of its features; thereafter, a brief explanation will be given of the reasons for each of these aspects.

The logic panel is of dimensions 12" x 14", .122" in thickness, and consists of 8 metal bus layers: 1) the component, or signal, layer; 2) a backplane layer, committed to -4.5 volts; and 3) 6 buried layers, all of which are dedicated either to ground, to -2 volts, or to -4.5 volts. The interstices between the metal planes are layers of conventional G10 epoxy filler. The spacing between the component side and the first buried layer, a ground plane, is 30 mils, to create a 75 ohm impedance for the signal traces on the component layer. The spacing layers between the other buried metal planes are each 10 mils

thick, thereby maximizing the interplane decoupling capacitance while maintaining sufficient thickness of the G10 epoxy to minimize pinholes and perforations and the possibility of short circuits between the planes.

Figure 29 also depicts a small portion of the component layout on the upper surface of the board; the complete array contains 192 32-pin leadless ceramic chip carriers and associated terminator networks and power plane decoupling capacitors. The array consists of 16 rows and 12 columns of leadless chip carrier subarrays, as well as fifteen 40-pin connectors along one edge of the board. The two edges of the board orthogonal

HIGH-FREQUENCY MULTILAYER CIRCUIT BOARD  
SUPPORTING WIRE WRAP INTERCONNECT  
OF SUBNANOSECOND ECL COMPONENTS  
ENCAPSULATED IN LEADLESS  
CERAMIC CHIP CARRIERS

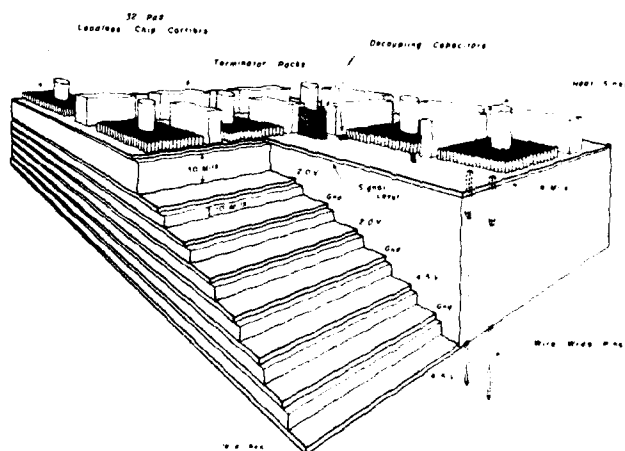


Figure 29

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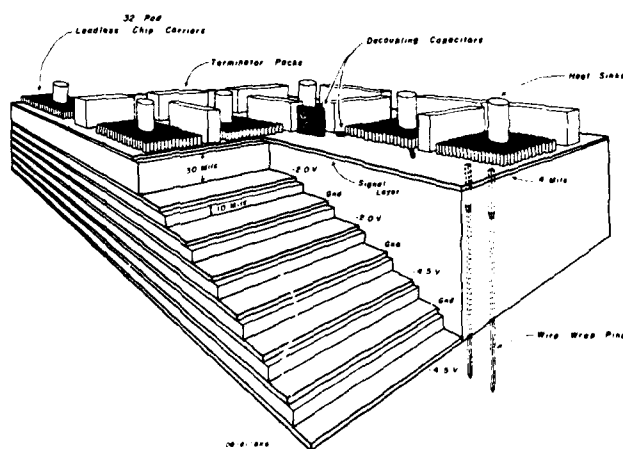


Figure 29

to the rows of connectors each contain two sets of power and ground studs; power is thus fed to the board along both of its long edges. Adjacent to the power and ground studs are four sets of specialized socketed structures designed to hold auxiliary components such as 300 mil or 400 mil dual in-line packages, specialized components such as DIP switches, or additional connectors. Each of the subarrays consists of a leadless chip carrier, surrounded on all sides by a transmission line terminator pack (these terminator packs will be described in a later section of the report). At the four corners of the leadless chip carrier are installed 3.3 microfarad high frequency tantalum electrolytic capacitors which help to decouple the -2 volt power planes to ground (the -2 volt bus is the most sensitive to the introduction of noise and crosstalk into the signal strings, as documented in the Year 1 Interim Report, Pages 69-71). In addition, small chip capacitors can be installed adjacent to the corners of each leadless chip carrier to assist in the decoupling of the -4.5 volt planes to ground.

A short foil trace 200 mils long on the printed circuit board conducts a signal from each castellation on the edge of the leadless chip carrier to a circular island. This island is the flush mounted head of a wire wrap pin which, by means of a plated-through hole, penetrates all layers of the board. The logic board wire wrap pins are headless, square cross section, machined brass pins plated with a gold-over-nickel layer;

no two pins are positioned closer than 100 mils. On the component side of the board, the foil trace continues over the top of the flush mounted head of the wire wrap pin and approaches one of the contact pads on the side of a terminator pack. If a termination is needed for a given signal pin, a small solder fillet joint is used to connect the board foil trace and the contact pad on the terminator pack. The terminator pack is held in position by two small wire posts which protrude from the underside of the terminator pack at either end. Ground and -4.5 volt or -2 volt bus connections, which must be supplied to each leadless chip carrier, are fed to the chip carriers by means of solid plated-through holes penetrating to the appropriate power and ground layers of the board.

The subarray patterns on the component side of the circuit board permit direct solder bonding of the leadless chip carriers, terminator packs, and decoupling capacitors to the board; alternately, chip carrier connectors can be installed on the same subarray on the logic board, soldered in place, and then accommodate the insertion of leadless chip carriers. If necessary, conventional 24-pin leaded flat packs can be installed in any subarray pattern in place of a leadless chip carrier. Considerable effort has also been expended to assure that this logic board will accept the installation of components which require signal, power, or ground attachments in "nonstandard" locations with an absolute minimum of special board preparation. Every one of the 32 padouts from the leadless chip carrier may be used as either a signal, power (either

2 volts or -4.5 volts, as required), or ground pin. Similarly, contacts on the terminator packs have been designed to match the power and ground feeds in the logic board so that no extra board preparatory work to commit ground is required, and only a small amount of board preparation to commit the appropriate power voltage for one type of infrequently used terminator pack.

With the above introduction to the features of the logic board in its present configuration, we will describe the experiments from which the final design of this board was derived.

#### Attempts to Achieve Dense Board Utilization

A major objective of this packaging study was the achievement of very high component densities on the logic panel, with the goal of at least 1.5 times that achieved in the dual in-line package board described in the Year 1 Interim Report. The studies of the electrical characteristics of wire wrap interconnects presented in the Year 1 Interim Report indicated that an extension of the wire wrap technique would perform very well for these boards as well; alternate methods do not allow such rapid fabrication of complete boards in a prototype development laboratory. The desire to exploit wire wrap technology was thus a major design constraint of this board. An alternate fabrication technique such as stitch weld would not be an improvement on a wire wrap technology, since stitch weld also has large interpin spacing requirements and demonstrates poorer

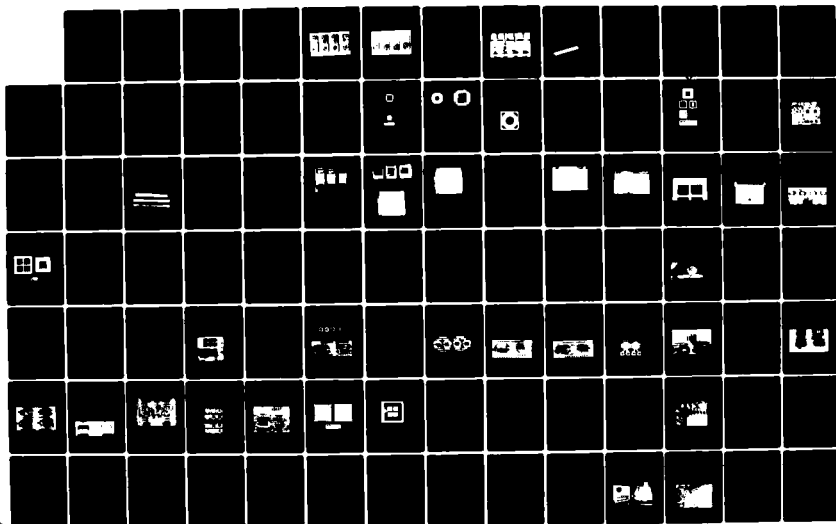
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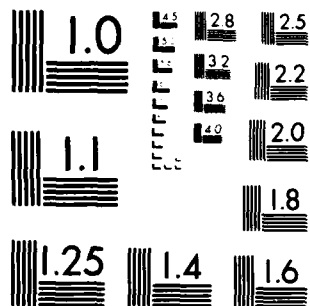
LEADLESS CHIP CARRIER PACKAGING AND CAD/CAM-SUPPORTED  
WIRE WRAP INTERCONN..(U) MAYO CLINIC ROCHESTER MN  
SPECIAL PURPOSE PROCESSOR DEVELOPMEN.. B K GILBERT  
NOV 81 AFWAL-TR-81-1206 F33615-79-C-1875 F/G 9/1

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MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-A

electrical performance than wire wrap at high frequencies (Year 1 Interim Report, Pages 6-7).

High component density had to be achieved for leadless chip carriers which were to employ a contact pad spacing of 50 mils, in spite of the fact that the physical constraints of wire wrap pins would not allow their installation on less than 100 mil centers. It was also determined that pinout spacing on the terminators would also have to be 100 mils if contact pins were used, but could be decreased to approximately 80 mils if contact pads were used. Lastly, the requirement for high value decoupling capacitors of nontrivial physical size also complicated the board design. In a pinless multilayer printed circuit board, employing buried layer resistors, layout constraints may be less stringent; however, as described earlier, multilayer printed circuit boards are unique designs, an approach considered unacceptable for a rapid prototype and fabrication capability.

The possibility was considered that special wire wrap pins of small diameter might be installed on less than 100 mil centers, thereby requiring a wire wrap bit capable of wrapping pins on less than 100 mil centers, and very small diameter pins. Gardiner Denver Corporation, a manufacturer of wire wrap equipment, was queried regarding the possibility of manufacturing wire wrap bits capable of wrapping pins on less than 100 mil centers. This vendor replied that the present bits are made up

of hardened alloy steel to allow minimum wall thickness; it appeared unlikely that bits with even thinner barrels could be manufactured at acceptable cost.

Information was requested from Augat, Inc., concerning the possibility of manufacturing very small hardened steel pins which could then be installed in a logic board at less than 100 mil spacing. Since the present pins are manufactured of machined brass with a gold-over-nickel plating, it was deemed unlikely that steel alloy pins of considerably smaller size could be manufactured because of the difficulty of machining steel alloys at reasonable cost; it also appeared unlikely to the vendor that the mechanical properties of the materials used for manufacture of printed circuit boards, e.g., G10 epoxy, polyimide, Kevlar, etc., would be able to maintain structural integrity with pins spaced on less than 100 mil centers.

Augat did comment, however, that packing density on the board could be increased by substituting for their standard socketed wire wrap pin (used extensively in the dual in-line package board reported in the Year 1 Interim Report) a special headless pin which they would be willing to design and fabricate for this project. The cross section of the upper end of the headless pin could be reduced to approximately 25 x 33 mils, in comparison to the circular end diameter of the socketed pins (which are flared to accept the pins of dual in-line packages) of 72 mils.

This suggestion led to the consideration that headless pins might be flush mounted in the board, allowing a pin to be positioned under alternate contact pads along the edges of each leadless chip carrier, or positioned under and solder bonded to a foil trace; either approach would make double use of the foil trace real estate. The positioning of headless pins under alternate chip carrier pads was abandoned because the vendor could not absolutely guarantee that all pins would be either flush or recess mounted, due to normal manufacturing tolerances. However, it did appear feasible to colocate flush mounted wire wrap pins and the foil traces, with the pins penetrating the logic panel through plated-through holes. Augat stated that they had never performed such an operation but would attempt to do so.

The results of the Augat fabrication study are depicted in Figures 30, 31, 32, and 33. Figure 33 shows a small experimental board which was fabricated by Augat using a modified headless wire wrap pin. Although pins were flush mounted into all of the test holes, only half of the pins were then soldered to facilitate inspection of the results of the flush mounting operation. Figure 30 depicts the flush mounted surface of the pins prior to solder bonding to the plated-through hole. Small solder shavings spalled from the lining of the plated-through holes during the insertion process may be observed in the holes. Figure 31 shows the slightly recessed pins after the soldering

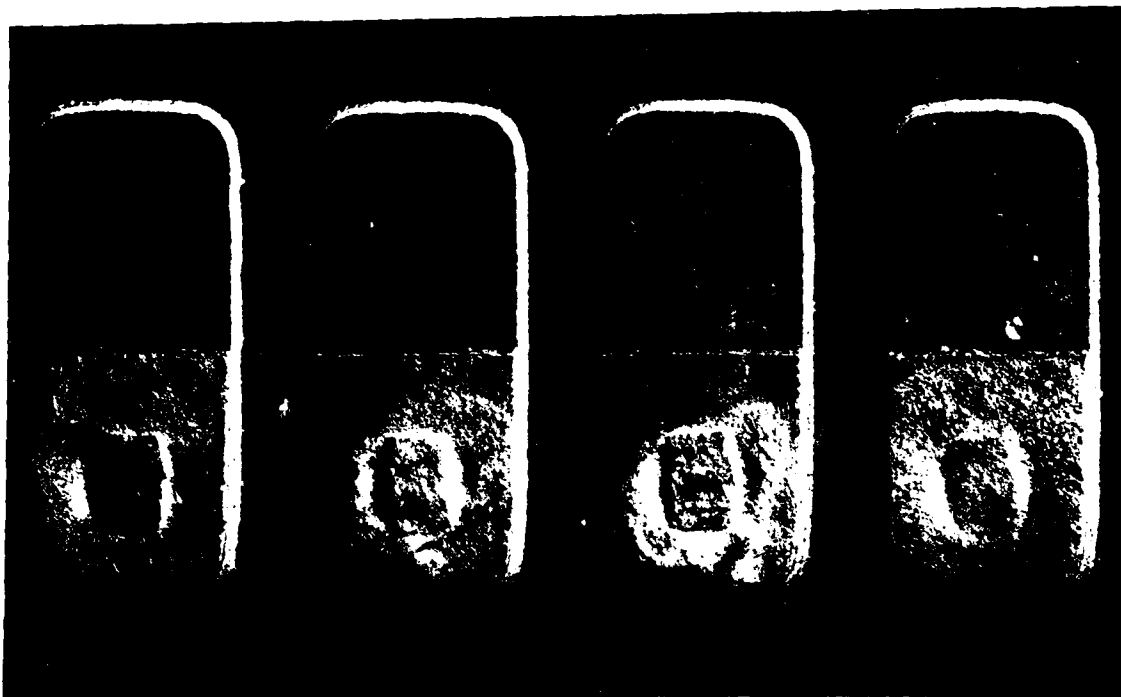
operation. The impression created by the photo is somewhat misleading; all pins are slightly recessed, an effect which is not altered by the soldering operation. Figure 32 shows the wire wrap side of the same pins as they protrude from the plated-through holes following the soldering operation. The solder bond is smooth; in addition, a sufficient guard band spacing, approximately 200 mils, exists between the upper portion of the solder bead and the maximum depth to which a wire wrap bit must extend during the wire wrapping process. These tests clearly



PHOTOMICROGRAPH OF HEADLESS WIRE WRAP PINS  
FLUSH MOUNTED IN PLATED-THROUGH HOLES.  
NOTE SHAVINGS OF SOLDER IN HOLES CAUSED BY  
PIN INSERTION SHEAR FORCES.

Figure 30

indicated that thousands of modified headless wire wrap pins could be inserted into a large multilayer circuit board and reflow soldered, i.e., that the logic panel would be manufacturable. In addition, the headless wire wrap pins will be much less expensive than the socketed pins used in the prior board design effort, which should partially offset the costs of the multiple layers and numerous plated-through holes required in the new logic panel.



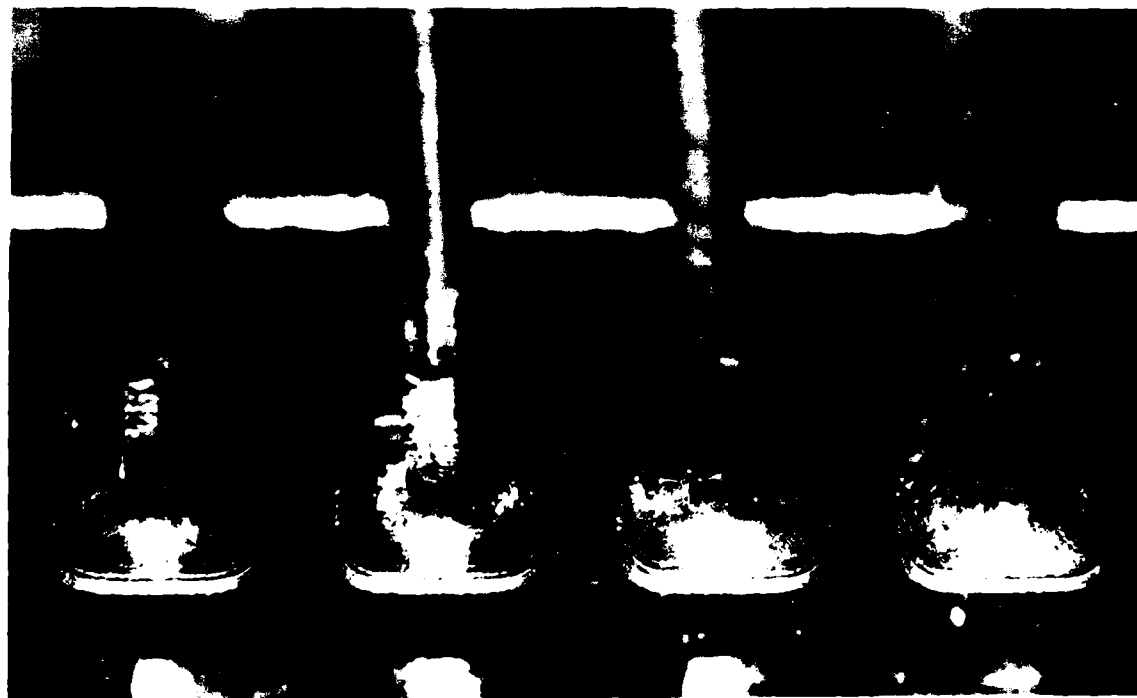
PHOTOMICROGRAPH OF FLUSH MOUNTED LEADLESS  
WIRE WRAP PINS AFTER REFLOW SOLDERING WITH  
SOLDER CREAM. NO PIN HEAD PROTRUDES ABOVE SURFACE.

Figure 31

The fabrication details and layer structures used in the new logic panel have undergone numerous design revisions. Following the pattern of the dual in-line package ECL board reported in Year 1, it was assumed that the new board would contain a ground layer, a -2 volt bus layer, and a -4.5 volt bus layer. However, the requirement for signal traces to interconnect the pads of the leadless chip carriers, the terminator attachment points, and the flush mounted wire wrap pins in turn necessitated a fourth, or "signal" layer. It was then necessary to compute the number of discrete layers which would have to be committed to each of the three power busses. Although all portions of the signal layer not committed to signal traces are committed to ground, this small grounded foil area is insufficient to constitute a satisfactory ground plane; as a conservative design approach, the ground foil on the signal plane was not included in the overall foil area calculations.

The design goal was a total foil area for each bus which, computed on a "per-dice" basis, would be no less than that employed in the dual in-line package (DIP) board described in the Year 1 Interim Report. Since the average density of ECL dice per unit area on the new leadless chip carrier board would be higher than for the DIP board, it was apparent that two or more metal layers in the board would have to be committed to each of the power busses, appropriately interconnected at numerous locations by solid vias. Calculations based upon the chip

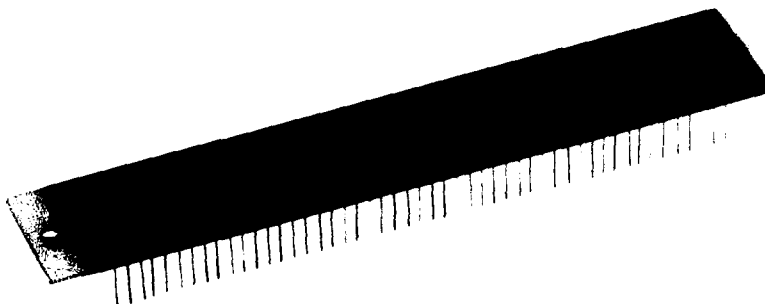
carrier footprint and layout of the signal plane, including the positive and negative impacts of the various vias on each bus, demonstrated that a total of seven bus layers and a signal layer would be required, with an alternation of layers as depicted in the artist's conception, Figure 29. These calculations accounted for the total area of each layer and for the average path width in both the x and y coordinates of the board; since no single metric adequately characterizes the foil area and hence the electrical behavior of the board, all three were employed to assess the number of busses incorpor-



WIRE WRAP SIDE VIEW OF FLUSH MOUNT PINS  
AFTER REFLOW SOLDERING. NOTE SMOOTH SOLDER  
BOND AT PIN-BOARD INTERFACE.

Figure 32

The reasons for taking these precautions with the bus layer design were outlined in the Year 1 Interim Report, Pages 69-71. Briefly, the impedance of the return current paths must be minimized wherever possible. The self inductance of an individual foil trace is approximately 2-10 nanohenries per lineal inch; the return path currents which flow through the power and ground layers contain frequencies over a range of 0.5-1 GHz for the fundamental up through harmonic components as high as 7-10 GHz. Data presented in the Year 1 Interim Report demonstrated that the self inductances of the power and ground planes may thus generate series impedances of 30-60 ohms per inch, and voltage drops of several hundred millivolts per inch, thereby destroying the voltage uniformity and stability of the power planes and



EXPERIMENTAL BOARD FABRICATED BY AUGAT  
TO DETERMINE FEASIBILITY OF FLUSH  
MOUNTING LEADLESS WIRE WRAP PINS

Figure 33

the noise margins of the operational circuits (Pages 63-71 of the Year 1 Report). With the higher packing density of the leadless chip carrier board in comparison to the DIP board, higher return path current densities per unit area must be accommodated. It was thus necessary to provide more AC ground return paths and more decoupling decapacitance between the individual power and ground layers than in the dual in-line package board; the metric of plane area per unit dice was employed to compute the values listed in Table 2. To assure maximum current carrying capacity, the metal layers will be etched from two ounce copper sheet, and backplated to 3 ounce thickness.

## 2. Selection of Board Substrate Material

The selection of substrate material for the logic panel was driven by conflicting constraints. Ease of fabrication was required to minimize unit board costs. Second, it was desired to maximize the dielectric constant of the board material to assure maximum decoupling capacitance between the power and ground plane layers. This approach is in contradiction to the constraint in multilayer printed circuit boards, in which a board material with the minimum possible dielectric constant is desirable to minimize the propagation delay of the buried stripline signal interconnects. Since the wire wrapped signal interconnects in the Mayo boards will

TABLE 2

POWER PLANE AND GROUND FOIL AREA COMPARISONS BETWEEN  
THREE-LAYER DIP BOARD AND EIGHT-LAYER LEADLESS CHIP  
CARRIER BOARD FOR SUBNANOSECOND ECL COMPONENTS.

ALL VALUES NORMALIZED TO PER-CHIP AREAS

	Ground Bus	-2 Volt Bus	-4.5 Volt Bus
DIP Total	.640	.779	.774
Foil Area, In <sup>2</sup>			
LCC Total	1.56	1.12	1.12
Foil Area, In <sup>2</sup>			
LCC %	140	43	44
Improvement			
DIP X-Dimension	.25	.525	.525
Foil, In			
LCC X-Dimension			
Foil, In	.735	.520	.520
LCC %	194	-1	-1
Improvement			
DIP Y-Dimension	.4	.4	.4
In <sup>2</sup>			
DIP Y-Dimension	.585	.580	.380
In <sup>2</sup>			
LCC %	46	45	-5
Improvement			

not be affected by the dielectric constant of the board substrate, the board material and layer thickness can be selected to maximize the capacitance and hence the noise decoupling between power planes. However, by adjusting the thickness of the first dielectric layer, it was possible to maintain a uniform 75 ohm impedance for the signal traces on the component side of the board.

The selection of board substrate was also constrained by its coefficient of linear thermal expansion; there is considerable evidence that direct solder bonding of leadless ceramic chip carriers to a logic panel of nonvitreous material can fracture the solder bonds because of differences in physical expansion of the board and carriers over a range of operating temperatures.

The following four materials were investigated for possible use in these logic panels. Conventional G-10 epoxy, with a dielectric constant of 4.1-4.6, is one of the most widely used and thoroughly understood board substrate structures. The material can be applied in very thin layers and will support a high density of vias and very thin trace widths. The peeling strength of the interface between the copper traces and the epoxy board is high, thereby minimizing accidental detachment of thin traces on the board. Conversely, the linear coefficient of thermal expansion of conventional G10 epoxy of 18 ppm/°C is approximately three times that of 94% alumina at 6.4 ppm/°C;

severe temperature cycling of a board could thereby result in stress cracking of solder bonds. However, the data of Fennimore\* including graphs of ranges of coefficients of expansion and physical strength of various materials as a function of temperature, indicate that for small alumina leadless chip carriers of approximately 500 x 500 mil outer dimensions or less, stress cracking is not a problem over at least 200 standard thermal cycles ( $-65^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ).

Polyimide was also examined in the light of the same constraints. The dielectric constant of polyimide is 4.0-4.4, very similar to that of epoxy. Polyimide can be applied in layers as thin as 4 mils, with good surface integrity (i.e., a minimum of surface defects and pinholes); however, the extra expense of applying very thin layers of polyimide to increase the interplane capacitance did not appear to be worthwhile. The board vendor also pointed out that the polyimide/copper trace interface is much less resistant to peeling than the copper/G-10 interface, thereby increasing the likelihood of inadvertent surface trace damage for a polyimide board. In addition, the entire structure of the board must be at approximately 125 mils thick in order to provide rigidity for a board of 12 by 14 inch dimensions. The vendor questioned the bending moment resistance of a polyimide board of these dimensions;

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\*Fennimore, J. E.: Using leadless components technology on printed wiring boards. Electronic Packaging and Production, December 1978, pp 128-132.

insufficient bending stiffness could result in cracks and fractures in the signal layer and within the inner metal planes of the board.

Teflon, with a dielectric constant of 2.0, was also examined in a similar manner. Fabrication problems with multi-layer Teflon boards are well known, particularly in regard to dimensional stability and rigidity, as well as resistance to bending moments. Teflon is usually exploited for its low dielectric constant and concomitant increase in stripline propagation velocity, usually demonstrating a 7-10% speed improvement over microstrip in alternate substrates such as G-10 or polyimide. However, to reiterate, interconnects on the proposed Mayo wire wrap board were to be by wire wrap, which is not affected by the board material. The negative features of the material, including its cost, difficulty of manufacture, and dimensional instability, allowed this material to be rejected almost immediately.

The next material examined as a board substrate was Kevlar, a relatively new aramid resin with unique physical and mechanical properties. Kevlar is so strong and resilient, with such a high damping coefficient, that it has been used successfully in the manufacture of downhill racing skis. The cured material is also extremely difficult to work, since it rapidly dulls cutting tools and thus resists penetration by small high-speed drills. The dielectric constant of Kevlar

is in the range of epoxy and polyimide; its primary significance in the context of this work is the rough equivalence of its linear coefficient of thermal expansion with that of 94% alumina. This single factor compels a consideration of Kevlar in any board designed for solder bonded leadless ceramic chip carriers. Several vendors have developed the techniques for working with Kevlar, including the use of high energy laser drills in place of conventional machining techniques; these exotic manufacturing techniques increase the cost of Kevlar boards in comparison to alternate materials.

Unfortunately, Kevlar is hygroscopic; that is, it absorbs large quantities of water vapor into the structure of the material, which in turn is followed by dimensional changes; such alterations could be crucial if very thin layers of this substrate are used, particularly if the layers are penetrated by large numbers of via holes. It is our understanding that at present manufactured boards must be surface sealed to prevent moisture absorption or must be stored under special low moisture conditions to maximize their shelf life. Although consideration of Kevlar has not been totally rejected, its negative features appeared in this first design effort to outweigh its advantages; however, further investigations of Kevlar will be undertaken for later design studies.

The increasing requirement for a board material which is easy to work, has acceptable electrical and mechanical

properties, with a linear coefficient of thermal expansion approximating that of 94% alumina, has motivated several attempts by materials vendors to develop board materials which will have a linear coefficient of thermal expansion similar to that of alumina. Materials examined to date include epoxy/Kevlar, titanium, copper/Invar, and alloy 42 in a sandwich configuration. These developments will be monitored by the Mayo group; such a material could provide a substrate with a nearly optimum combination of electrical, thermal, and mechanical characteristics necessary for boards employing ceramic leadless chip carriers. If such a material becomes available, a refabrication of the current board design using the new material will immediately be considered.

## SECTION VI

### TECHNIQUES OF BONDING LEADLESS CERAMIC CHIP CARRIERS TO MULTILAYER WIRE WRAP CIRCUIT BOARDS

#### 1. An Investigation of Leadless Chip Carrier Connectors

A major advantage of the dual in-line packages and socketed wire wrap boards described in the Year 1 Interim Report is the ease of installing integrated circuits in the logic panel by manual or automated insertion techniques, and the equivalent ease of manual replacement of damaged components. The feasibility was therefore investigated of a socket for leadless chip carriers which could be soldered en masse to a board substrate, with later direct manual insertion of components. Given the high operating frequencies of the subnanosecond ECL dice, assurance was required that candidate sockets or connectors for leadless chip carriers would not themselves degrade performance of the ECL dice. In addition, such connectors would have to be capable of dissipating large quantities of heat generated by the subnanosecond ECL dice.

As described earlier, the small leadless chip carrier presently completing design is only the first of a small family of chip carriers covering the range from approximately 32 pins to 180-200 pins; hence, the Mayo-conducted review of feasible

chip carrier connector designs was extended to include components from 32 pads to 200 pads. It soon became apparent that there were actually two separate sets of technological problems in the development of leadless chip carrier connectors, one relating to connectors for small leadless chip carriers (approximately 500 x 500 mil edge dimensions) and a second in the design of connectors for medium and large carriers.

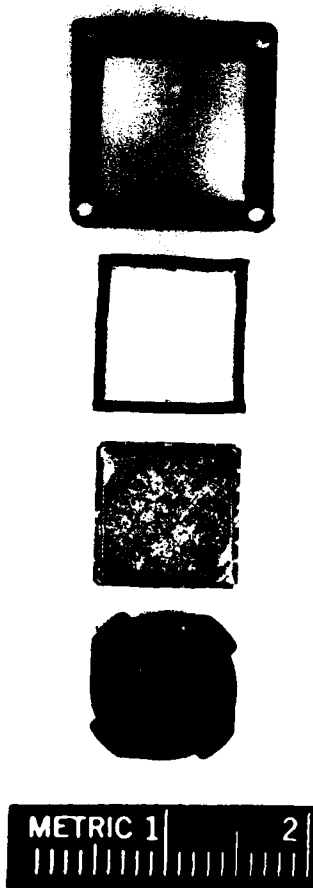
Assuming a center to center pad spacing for all chip carriers of 40 mils (military) or 50 mils (commercial), several candidate manufacturers of chip carrier connectors stated that the design problems for small chip carrier connectors were proportionately greater than those for the medium and large connectors. Regardless of the pad spacing on the carrier, there is a minimum structural dimension overhead which is independent of the size of the chip carrier connector; this irreducible minimum is an unacceptably large percentage of the connector edge dimension for the small chip carriers. It was possible to identify only two designs for small chip carrier connectors, both of which have been examined in this study. Also investigated was a third potentially feasible technique for small leadless chip carriers, relying on a design pioneered by Tektronix, Inc., for analog circuitry interconnects.

Technit, Inc. proposed a small chip carrier connector for the 3M Corporation 88 ST-524AC 24-pin ceramic leadless chip carrier which was used in the early operational verification tests discussed in the Year 1 Interim Report (Pages 92-97). Although

the Technit connector was designed for cavity-up mounting of the chip carrier, this problem could have been circumvented by a chip carrier redesigned for lid-down mounting such as the new Mayo-designed carrier described earlier. In the Technit approach, small strips of silicone rubber are manufactured which are penetrated by axially aligned tiny wires; small pieces of this material are bonded to a silicon rubber support structure or inserted into slots in the connector such that the long axes of the embedded wires are orthogonal to the plane of the logic board (Figures 34, 35, and 36).

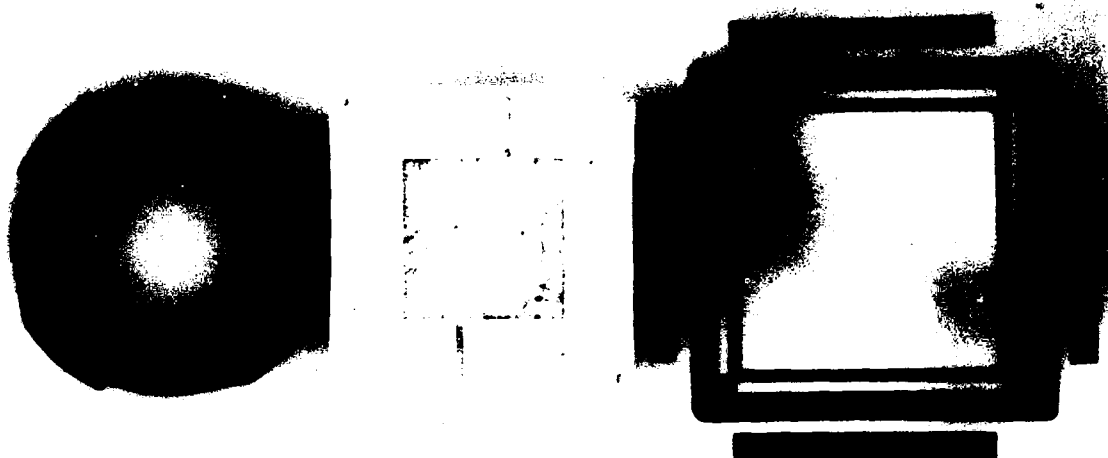
The chip carrier is then inserted into the connector, and is compressed onto the silicone strips by a twist-lock lid. The strips deform under this pressure such that the upper ends of the multiple fine wires supposedly make contact with the pads on the leadless chip carrier and the lower ends with contact pads on the logic board. Since the axial wires are insulated from one another and are spaced at approximate intervals of 1-2 mils, some will contact a pad on the leadless chip carrier, while others will be in the guard band between adjacent pads on the chip carrier, thereby creating a dead or insulating band which prevents short circuits between adjacent pads on the chip carrier.

A small printed circuit board was designed to match the Technit connectors; the connectors were installed on the board, and a leadless chip carrier with an F100102 ECL dice



TECHNIT 24-PAD CHIP CARRIER CONNECTOR  
SHOWING WIRE IMPREGNATED SILICONE RUBBER CONTACTS,  
CHIP CARRIER, AND LID

Figure 34



TECHNIT CONNECTOR FOR 68-PAD  
JEDEC TYPE A LEADLESS CHIP CARRIER

Figure 35

was inserted. DC and AC operational tests were then attempted on the chip carrier and connector combination. Even DC contact between the chip carrier and the logic board could not be reliably established. The pressure on the chip carrier applied by the lid could not be made uniform over all edges of the chip carrier, resulting in insufficient pressure at some edge segments of the chip carrier and too much pressure in other regions. Excessive pressure created sufficient deformation of the silicone rubber to distort the embedded wires into a partial hair-pin shape, preventing contact with either the chip carrier or the board contacts. Even when appropriate electrical contact

could be made for power and ground, the voltage drop across the contact points was so high that an undervoltage condition on the chip power and ground inputs was always present. After several attempts to rectify these problems, this chip carrier connector design was abandoned.

The second candidate for a small chip carrier connector examined a system developed by AMP, Incorporated, comprised of a plastic chip carrier connector and a specially designed mass producible nonhermetically sealed plastic leadless chip carrier intended for extremely low cost, high density applications. As a substitute for a (costly) hermetic seal, a low



TECHNIT CONNECTOR FOR  
68-PAD JEDEC TYPE A LEADLESS CHIP CARRIER  
SHOWN IN ASSEMBLED FORM

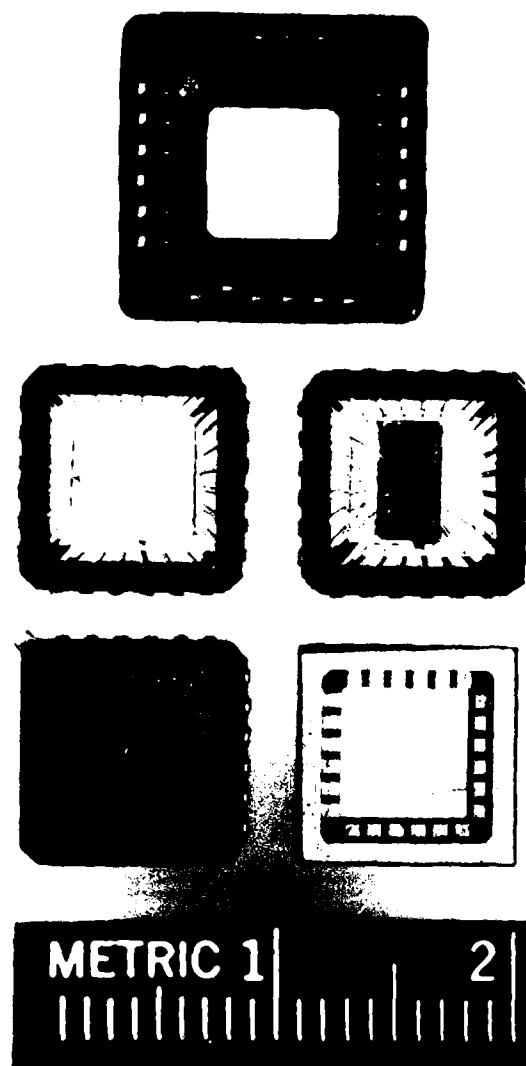
Figure 36

cost inert silicone gel is injected into the chip carrier after installation and wire bonding of the integrated circuit. Since these chip carriers and connectors are intended for low power TTL and MOS parts, no attention has been given to the removal of large quantities of heat from the chip carrier; similarly, since the low power devices also have very slow logic rise and fall times, no attention has been given to the electrical performance and electrical parasitics in either the chip carrier or its connector. Figure C-1304-81A depicts an empty chip carrier connector, an empty chip carrier prior to insertion of the silicon dice, a chip carrier with the silicon dice installed but prior to injection of the silicon sealant, and the chip carrier with the nonhermetic lid installed. Also depicted is a small ceramic leadless chip carrier with the same edge dimensions, which will be discussed below.

Both the plastic chip carrier and the plastic connector are designed with keyways which prevent incorrect installation of the chip carrier. It is thus impossible to invert the chip carrier in the connector to position the silicon die at the top surface of the connector, thereby defeating the ability to air cool the chip carrier. Representatives of AMP, Incorporated, indicated that a redesign of the tooling for the plastic chip carrier and its connector would be required to allow inverse mounting; the plastic encapsulation would nonetheless prevent efficient heat transfer from the carrier.

Because many potential users of the combined chip carrier and connector of Figure 37 are reluctant to use a nonhermetically sealed plastic chip carrier, even though willing to consider an inexpensive plastic chip carrier connector, AMP teamed with Ceramic Systems, Inc., to develop a small high quality 24-pin leadless ceramic chip carrier which can be installed lid-up into the AMP plastic leadless chip carrier connector. This combination appeared worthy of consideration, provided only that the carrier or connector could be modified for lid-down mounting.

Consultation with both vendors concerning this possibility uncovered an irresolvable contention situation. Both the AMP carrier connector and the Ceramic Systems leadless chip carrier are designed with keyways which prevent lid-down insertion of the chip carrier in the connector. It appeared that a "simple" change in the design of the carrier connector would easily allow inverse mounting of the chip carrier. AMP, Inc., refused to consider this alteration, stating that such a change would create the possibility of component installation errors. AMP suggested a "simple" change in the design of the chip carrier to permit inverse mounting. This suggested change was discussed with Ceramics Systems, who pointed out that the proposed modification to the chip carrier would threaten the quality of its hermetic seal. Although these alterations could certainly be carried out with the cooperation of the vendors, additional



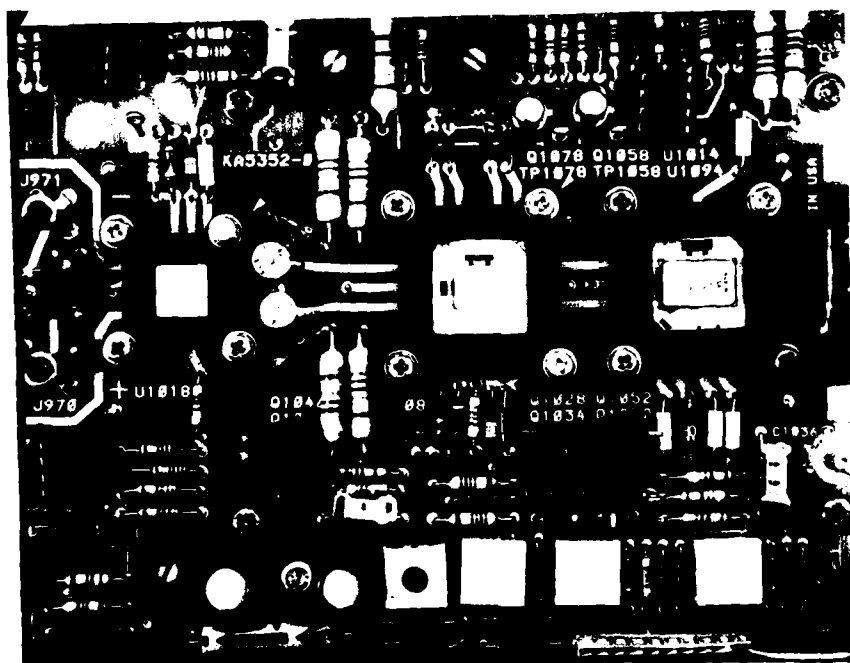
AMP CORPORATION 24-PIN NONHERMETIC PLASTIC  
CHIP CARRIER AND CONNECTOR WITH  
CERAMIC SYSTEMS CORPORATION LCCC

Figure 37

information presented below suggests that chip carrier connectors may not be suitable for ultra high frequency applications and do not justify the cost of this change.

A third possible connector investigated for small, medium, or large chip carriers is based upon a technique developed by Tektronix, Inc., for reflection-free high frequency sockets for analog hybrid integrated circuits. These connectors, shown in Figure 38, are used in the high frequency preamplifiers of the Tektronix 7104 1 GHz oscilloscope. In this approach, a ceramic leadless chip carrier is solder bonded to a thin sheet of ceramic of uniform thickness whose edge dimensions are approximately three times that of the leadless chip carrier. Gold controlled impedance traces are solder bonded to the contacts on the leadless chip carrier; the signals then pass along the gold traces to the very edges of the thin ceramic sheet. The printed circuit board supporting the chip carrier is manufactured with a small well, the edge dimensions of which are exactly those of the ceramic slab, and the depth of which is uniform and equal to the thickness of the ceramic slab. When the slab is placed in the well, the top surface of the slab is exactly coplanar with the top surface of the circuit board.

Both the board and the slab carry controlled impedance traces whose ends meet at the edge of the well. Connection of the traces on the ceramic slab with those on the logic



TEKTRONIX FLUSH MOUNT AND STEPPED HYPCON CONNECTORS  
FOR HIGH FREQUENCY ANALOG CIRCUITS

Figure 38

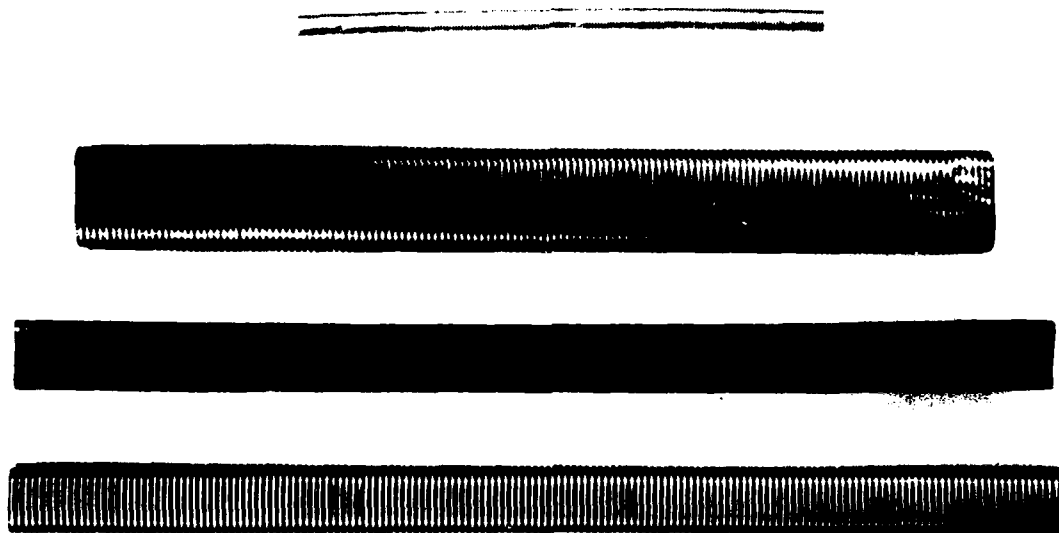
board requires a set of "shorting bars", in the form of a piece of silicone rubber whose bottom edge contains a set of parallel gold traces of the same width as the circuit board traces and approximately a quarter of an inch long. The silicone rubber pieces are, in turn, enclosed in a small hollow square compression-fit structure, grooved along its underside to hold the silicone rubber pieces, with provision for threaded mounting to the board at the corners of the compression structure. These "HYPCON" connectors have demonstrated, by time domain reflectometry, impedance discontinuity area products of less than 1 millirho nsec, thereby making them almost perfect high frequency sockets. Two styles of these HYPCON connectors have been developed: the unit described above, called a "flush mount HYPCON", and the "stepped HYPCON", which allows for some vertical misalignment in the planar surfaces of the substrate and the ceramic slab. The HYPCON connectors exhibit several stringent mechanical constraints: the depth of the well in the circuit board must be extremely uniform and well controlled, as must the thickness of the ceramic slab and the spacing of the traces both on the ceramic slab and on the printed circuit board. The traces must be separated by wide guard bands; only 16 leadouts are supported by each HYPCON connector.

Nonetheless, the HYPCON approach appeared so attractive that it was explored further at Mayo using alternate materials and potential fabrication techniques. Augat, Inc., stated that it would be difficult if not impossible to manufacture

very large circuit boards with large numbers of square or rectangular wells of precision depth. The possibility was then considered of placing the leadless chip carriers on the surface of the board and using a device such as a STEPPED HYPCON connector to bridge the gap between the contact pads on the leadless chip carrier and the foil traces on the logic board.

Several vendors were contacted who were purported to be manufacturing test lots of silicone rubber embossed with metal contact lines, including Technit, Inc., and AMP, Inc. The material was manufactured in flat surface sheets, with 10 mil foils spacing on 20 mil centers, and in cylindrical "worms" with the smallest structures employing 3 mil circumferential bands separated by 7 mil guard bands (Figure 39). Design of a suitable support structure (connector) was deemed to be a problem if the worms were used to create a fillet connection, since the 50 mil spacing between contact pads on the chip carriers and on the circuit board would make proper alignment very difficult even for a small leadless chip carrier if the silastic was required to bridge a lateral distance of about 150 mils and a vertical distance (the height of the chip carrier) of 75 mils. Note that the original exploitation of this bridging approach, the Tektronix HYPCON connector, used a pair of coplanar or nearly coplanar surfaces, a much coarser spacing between leads, many fewer leads, and only a few such connectors in each system; in addition, Tektronix regards the HYPCON as a very high cost connector usable only in selected applications.

The most feasible technique of using the closed loop metal ribbon covered silastic worm structures depicted in Figure 39 would employ sections of this material cut to an appropriate length and enclosed in a connector, where it would be squeezed between the surface contacts of the leadless chip carrier and the logic board, in a manner similar to that of the Technit connector described earlier. Either lid-up or lid-down mounting of the chip carrier could be used, provided only that appropriate contacts are placed on the surface facing the logic board.



COPPER/GOLD RIBBON COVERED SILASTIC WORMS

Figure 39

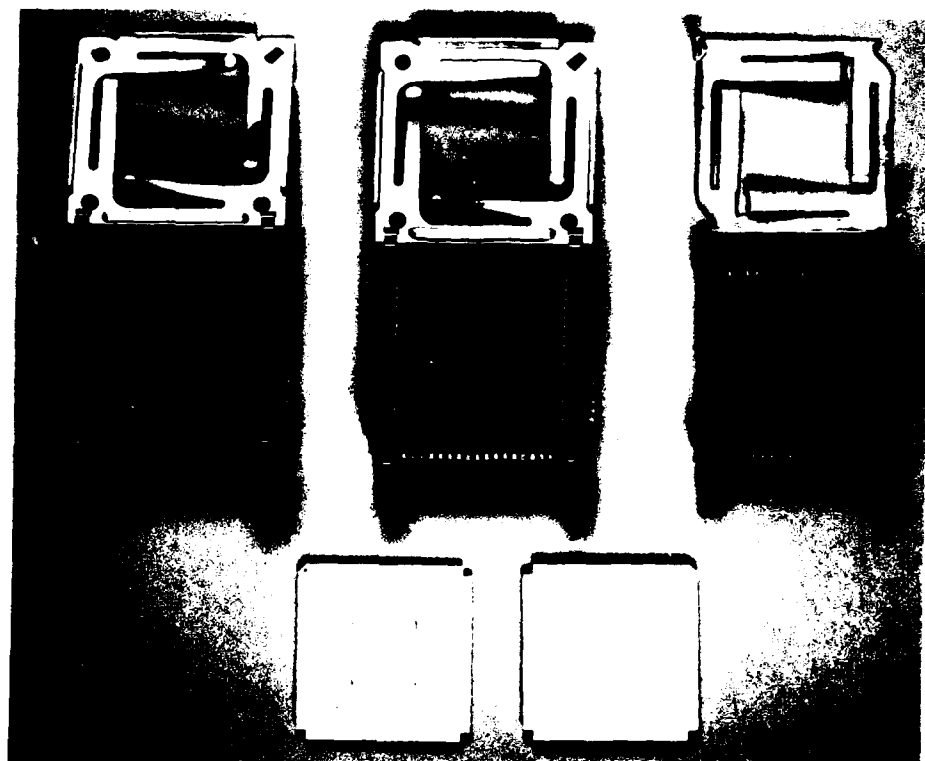
It would be necessary to assure that proper compression forces are exerted on the chip carrier and the conductive silicon cylinders by the lid and chip carrier connector; the difficulty of achieving proper contact pressure was a primary reason that the embedded wire and silicon connector proved unsatisfactory.

Nonetheless, the closed loop ribbon devices have a higher probability of success than Technit's embedded wire material. As may be observed in Figure 39, the quality of these foil wrapped silicone cylinders is extremely high. We were encouraged sufficiently to proceed with this examination, but have been prevented from doing so. The best quality silicon cylinders were manufactured by AMP, Inc., which apparently was having severe yield problems with the devices and as a result was experiencing excessive manufacturing costs. First AMP, and then Technit, suspended manufacture of these units pending improvements in yield and process technology. There is also a concern that because the conductors on the silastic worms are closed loops, self inductance effects of the loops, and the capacitance between adjacent loops, may make them unsuitable for high frequency operation. This concern could not be tested when the earlier studies were undertaken; however, recently purchased test equipment which was not available in Year 2 of this project will allow testing of these materials during Year 3 (July 1, 1981-June 30, 1982). As a result of our inability to evaluate these wire covered worms and the cessation of their manufacture, tests on this approach have been suspended temporarily.

## 2. Study of Chip Carrier Connectors for Medium and Large Size Leadless Chip Carriers

The number of vendors and unique designs for medium and large (68-200 pins) leadless chip carriers is greater than for small leadless chip carriers. Although the initial phases of this study are concerned with the small leadless chip carriers, the interconnection problem for medium and large size carriers must be solved for the high frequency environment as well; as a result, our review of chip carrier connectors also included those designed for the larger chip carriers. Most vendors have designed their initial connectors for the JEDEC Type A 68-pin leadless ceramic chip carrier, depicted in Figure 22.

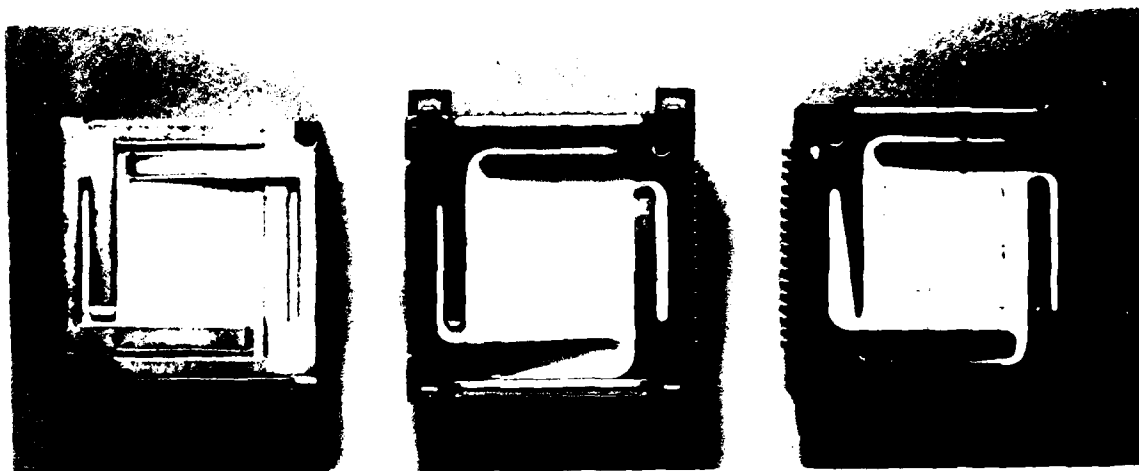
The first high quality connector which became available for these components was the ADS connector designed by AMP, Inc., and depicted in two versions in Figures 40 and 43. The first version, depicted in Figure 42, makes electrical contact with the circuit board by means of small solder tail pins in two rows on each edge of the connector; no interpin spacing is less than 100 mils. In the second version, electrical contact with the substrate circuit board is by means of small surface mount copper pads on the bottom of the chip carrier connector spaced on 50 mil centers in a single row on each edge of the connector (Figure 43).



AMP ADS CONNECTOR IN THREE VERSIONS FOR  
68-PAD JEDEC TYPE A LEADLESS CHIP CARRIER

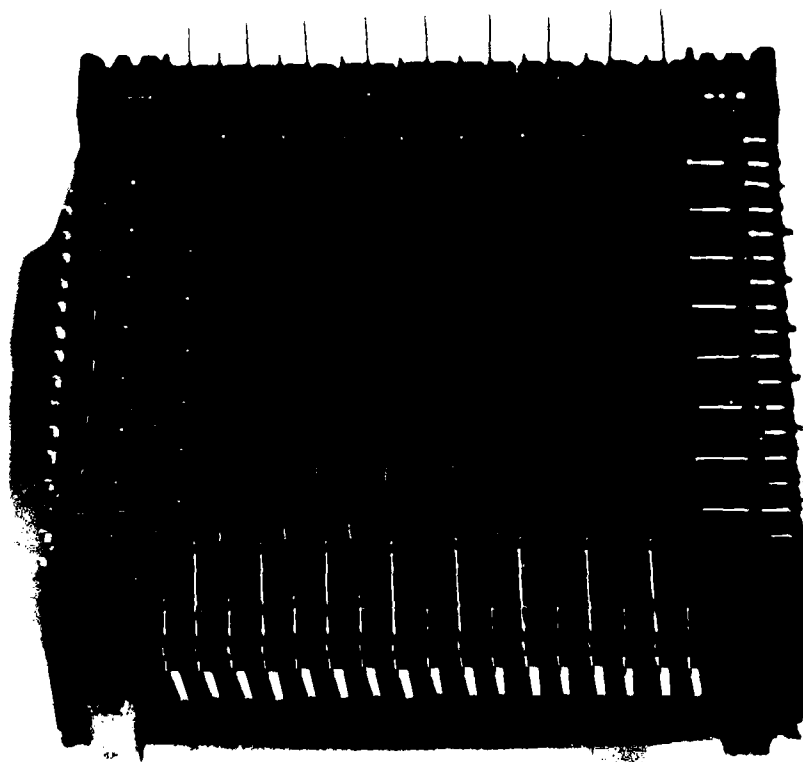
Figure 40

The mechanical and heat removal features of this chip carrier connector appear to be excellent. The chip carrier is mounted lid-down in the connector, with spring loaded metal fingers in the connector making a wiping-action positive pressure contact with the metal pads on the cavity side of the chip carrier (refer to Figure 22). In addition, the chip carrier connector employs an integral lid which is held in position by a pair of spring clip retaining bars; considerable pressure



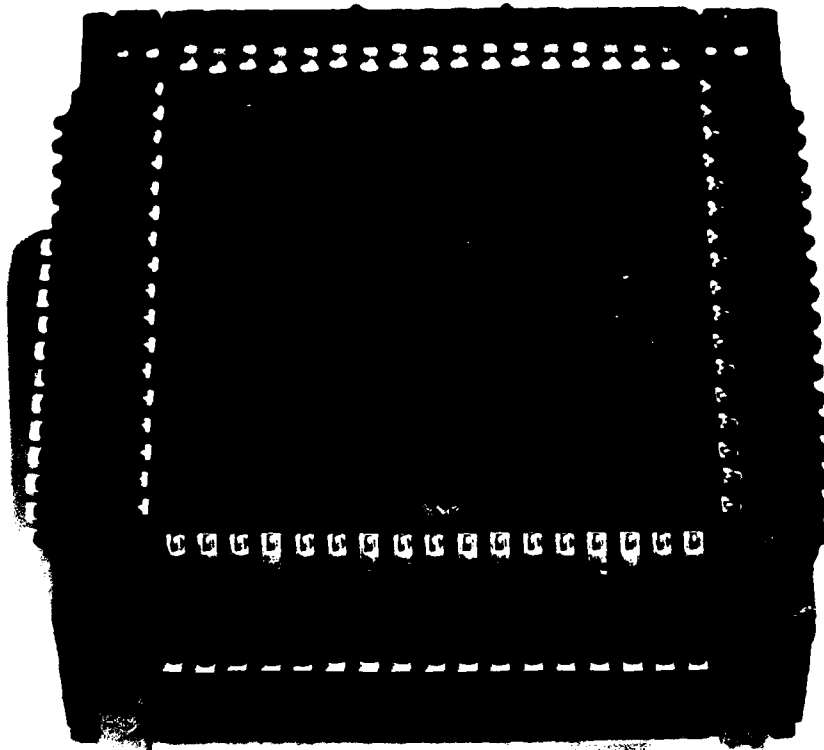
AMP ADS CONNECTORS SHOWN WITH 68-PAD  
JEDEC TYPE A LEADLESS CHIP CARRIER INSTALLED

Figure 41



UNDERSIDE VIEW OF SOLDER TAIL VERSION OF AMP ADS CONNECTOR

Figure 42



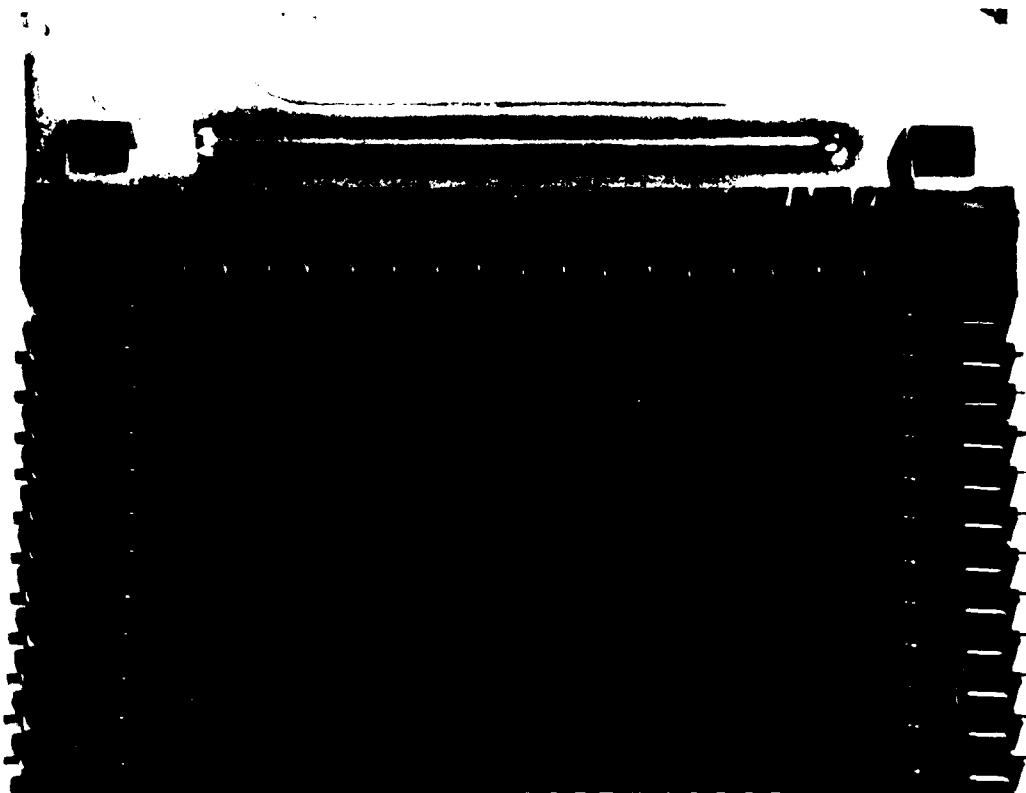
UNDERSIDE VIEW OF SURFACE MOUNT VERSION  
OF AMP ADS CONNECTOR

Figure 43

must be used to close the lid and force the chip carrier onto the connector contact pins. Since the lid is an arrangement of open metal fingers (see Figure 43), and since the center back area of the chip carrier is exposed to the air and not covered by the lid, heat removal to the ambient airstream with or without a copper heat stud is quite feasible.

Although further testing of this chip carrier will be performed in Year 3 of the research using newly purchased high frequency impedance measuring equipment, the vendor (AMP, Inc.) has stated that little attempt is made to control parasitic impedances, in the design and manufacture of the ADS connectors. Figures 44 and 45, photomicrographs of the interior of two versions of the chip carrier connector, illustrates that the metal contact springs, which are hairpin shaped, are coplanar with one another over their entire vertical run from the board surface to the bottom of the chip carrier itself. AMP, Inc., indicates that interelectrode capacitances of 10-20 pF, and capacitances between electrodes and ground of approximately the same magnitude should be expected, clearly an unacceptable level for environments in which more than 3-4 pF parasitic shunt capacitance is deemed to be too high. AMP is aware of the limitations of this ADS chip carrier connector for high frequency applications, and does not recommend its use with short risetime ECL devices. It is noteworthy, however, that AMP believes that the ADS connector design can be expanded to incorporate larger numbers of pins and larger chip carriers, perhaps up to 200 pinout locations, though the number of rows of contact pads on the chip carrier which could be accommodated remains an open question.

AMP, Inc., and Augat, Inc., have developed alternate designs for families of leadless chip carriers which are much simpler conceptually than the ADS connector, are more fragile,

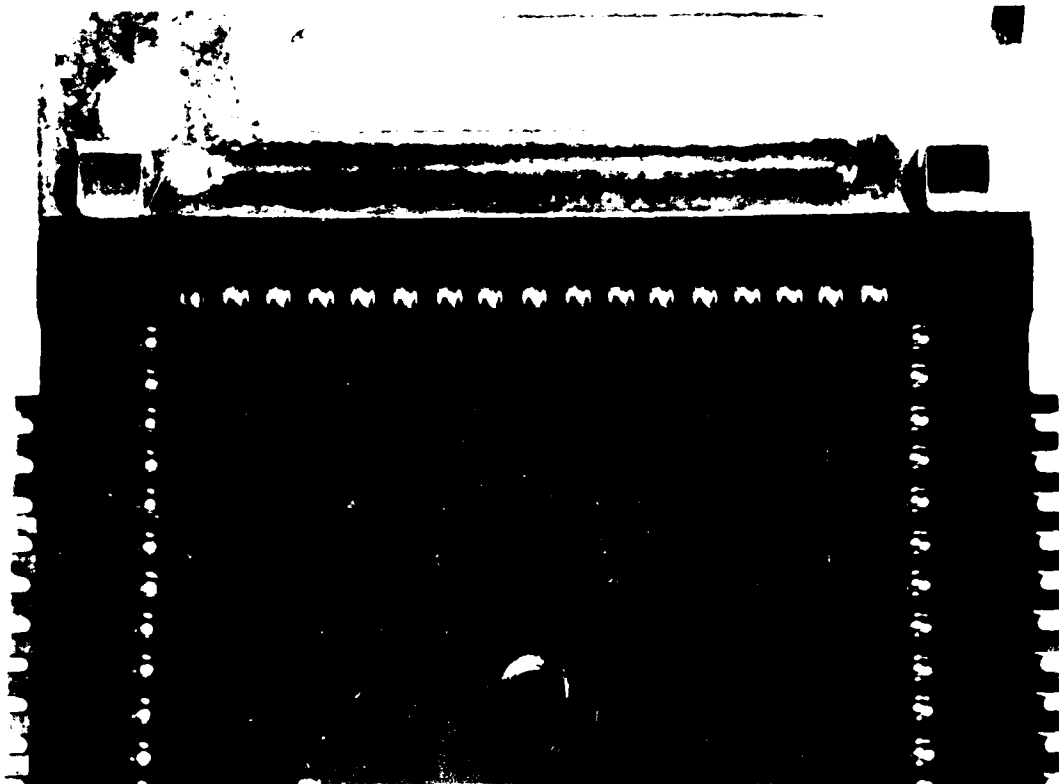


PHOTOMICROGRAPH OF CONTACT PINS IN THE  
SOLDER TAIL VERSION OF AMP ADS CONNECTOR.

NOTE HAIRPIN SHAPE OF CONTACT PINS.

Figure 44

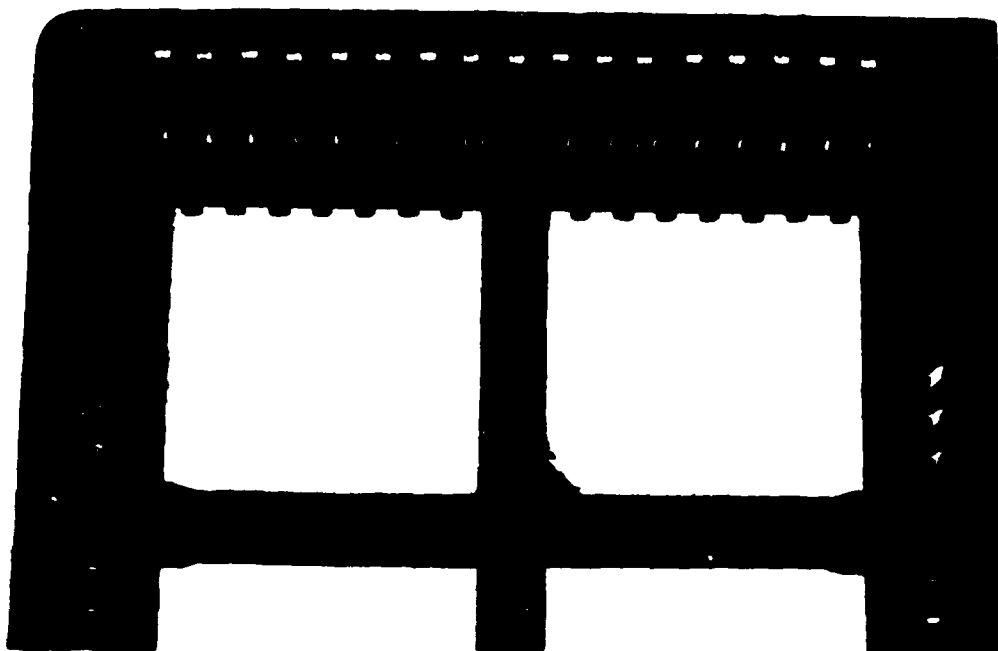
less costly, and which also appear to possess improved high frequency electrical characteristics. These connectors, which appear in Figures 46 and 47 employ a simple plastic body with very short hairpin-shaped contacts, and which do not have built-in test points along their edges as do the ADS connector. A simple spring clip arrangement serves as the holddown clamp for the chip carriers, which are inserted lid-down into the



PHOTOMICROGRAPH OF CONTACT PINS IN THE  
SURFACE MOUNT VERSION OF AMP ADS CONNECTOR.  
NOTE BULK AND HAIRPIN SHAPE OF CONTACT PINS.

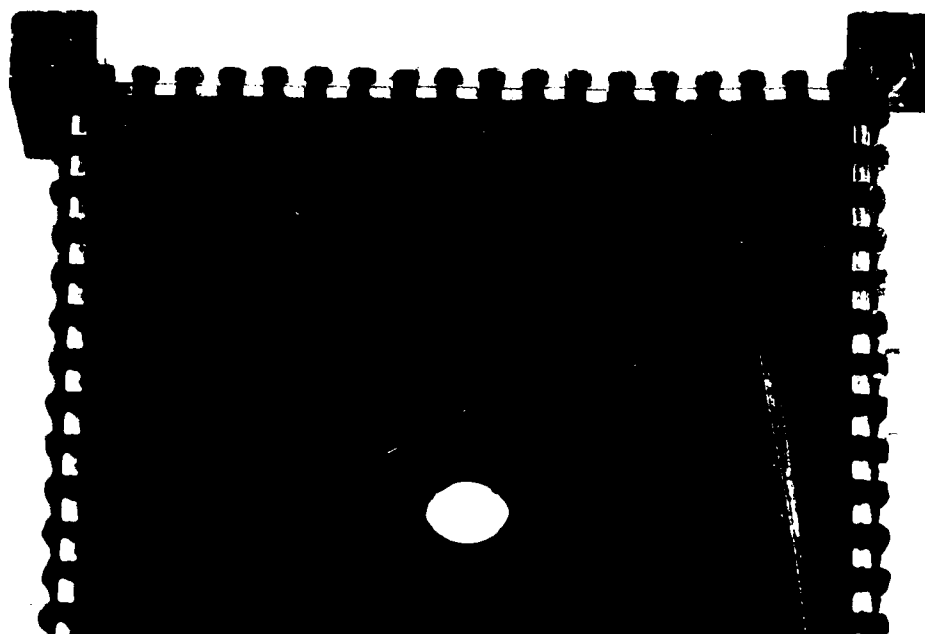
Figure 45

connectors. The metal content of these connectors is less than that of the ADS connector, which should result in lower parasitic impedances. Preliminary solder bonding tests have been performed with these new styles of chip carrier connector, but electrical performance tests await the delivery of



SIMPLIFIED CONNECTOR FOR JEDEC 68-PAD LEADLESS  
TYPE A CHIP CARRIER, MANUFACTURED BY AMP, INC.

Figure 46

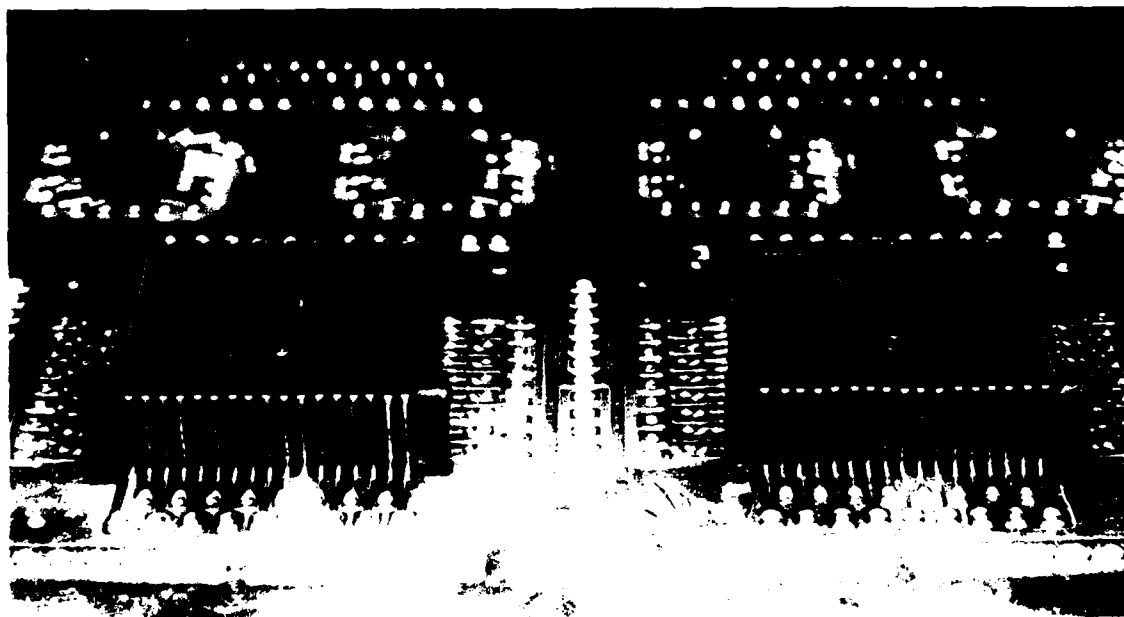


SIMPLIFIED CONNECTOR FOR JEDEC 68-PAD LEADLESS TYPE A  
CHIP CARRIER, MANUFACTURED BY AOGAP, INC., CONTACT METAL,  
AND HENCE PARASITICS, ARE MINIMIZED

Figure 47

the new high frequency impedance measuring equipment. Figure 48 shows that these connectors can be solder bonded to a circuit board manually or by vapor phase reflow techniques.

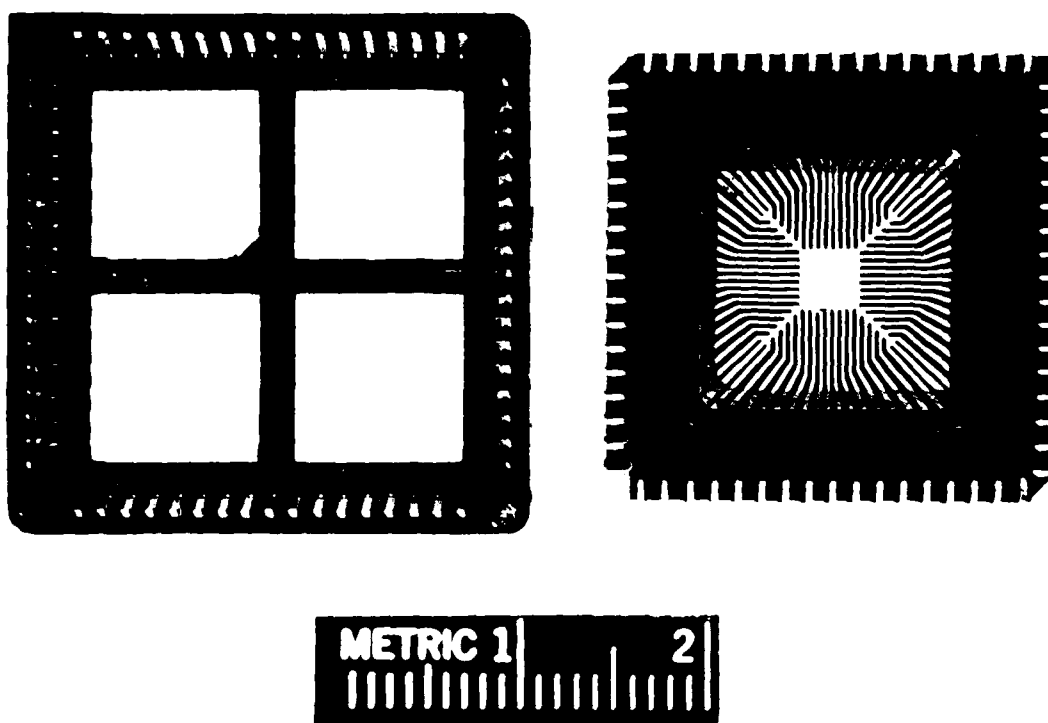
Until recently, these connectors have been available only in soft tool demonstration parts; the vendors have cautioned that the electrical characteristics of the test parts may not be identical to those of the finished hard tool parts. Neither vendor plans to manufacture such connectors for chip carriers containing less than 68 contacts, though larger connectors could be manufactured. These devices will be tested further and reported on in the Third Year Interim Report. Regarding the possibility of use of chip carriers for the small chip carriers, the only available candidate, the small inexpensive



AUGAT 68-PIN LEADLESS CHIP CARRIER CONNECTORS  
VAPOR PHASE REFLOW SOLDERED TO PRINTED CIRCUIT BOARD

Figure 48

plastic AMP connector, appears to be unsuitable for high frequency, high power dissipation environments. Figure 49 also shows that the AMP connector of Figure 46 also mates with a JEDEC 68-pad leaded Type A chip carrier, but the combination appears unsuitable for ECL components because of the large amount of metal in the contacts.



LOW COST AMP CONNECTOR FOR LEADLESS OR  
LEADED TYPE A JEDEC 68-PAD CHIP CARRIERS, SHOWN  
WITH COMPANION LEADED TYPE A CARRIER

Figure 49

### 3. Attachment of Leadless Ceramic Chip Carrier Directly to Circuit Board Via Solder Bonding Techniques

It was clear at the outset of this study that solder bonding of leadless chip carriers to substrate boards promised the best electrical connections, and, barring the problem of fracture cracks, the best mechanical attachment as well. A review was undertaken of the optimum solder alloy for this purpose and the optimum soldering approach, with the constraint that the bonding method must be useable in a system prototyping environment rather than a mass production environment; the costs of special equipment associated with the bonding method selected must be reasonable and suited to the fabrication of small numbers of logic boards. Ease of removal of components for replacement or modification had to be considered if solder bonding is employed, since soldered components are difficult to replace if system rework is required. Although the review of solder alloys was made in conjunction with the study of soldering methods, the two topics will be presented separately for clarity.

The standard, widely used 60% tin, 40% lead solder was investigated first, as well as a variant containing 62% tin, 36% lead, and 2% silver (Dupont 4499). This material has a melting point of 188° Centigrade, but a tensile strength of 7700 psi. This solder material is widely available, and can be plated directly onto logic boards in any desired thickness

during board manufacture, a capability which was exploited in the prototype board fabrication tests described below. A negative aspect of conventional tin-lead solder is its relatively high melting point which, though lower than silver or gold solders, subjects the integrated circuits to a relatively high thermal shock, particularly if automated, high temperature soldering approaches such as wave soldering are employed.

It appeared worthwhile to consider the use of solders comprised of low temperature eutectic alloys, whose melting temperatures ranged from 209° Centigrade for a solder composed of 50% indium, 50% lead, to 188°C for conventional 60-40 tin-lead solder, to 130°C for an alloy of 40% indium, 40% tin, and 20% lead (see Table 3). Note also that the tensile strengths of these solders range over a 2 to 1 margin, from 4,670 psi for 50% indium, 50% lead solder to 7,700 psi for conventional tin-lead solder. Clearly, the use of a solder with melting temperature of 130° C could create significantly less thermal shock to the chips and logic boards, provided that bonding temperatures could be maintained at just a few degrees above the fusion temperature of the solder selected.

Discussions with Indium Corporation of America revealed several problems associated with the use of unconventional eutectic solders. Most of the low temperature solders contain a substantial percentage of Indium, which significantly affects the wetting characteristics of the solder. Indium-based solders

TABLE 3

TENSILE STRENGTH AND MELTING POINTS  
OF VARIOUS SOLDERS

Indalloy Number	Temperature °C		Tensile Strength P.S.I.	Electrical Conductivity % of Copper	Composition
	Liquidus	Solidus			
290(E)	143	143	800	23.0	97In 3Ag
2	149	142	2500	13.0	80In 15Pb 5Ag
4	157	157	575	24.0	100In
204	174	160	3450	8.8	70In 30Pb
205	185	174	4150	7.0	60In 40Pb
60/40	188	183	7700	11.5	60Sn 40Pb
7	209	180	4670	6.0	50In 50Pb
206	225	195	5000	5.2	40In 60Pb
10	264	250	5450	4.6	25In 75Pb*
150	280	270	5550	4.5	19In 81Pb*
164(MP)	300		4560	5.5	5In 92.5Pb 2.5 Ag*
DUPONT 4499	189				62Sn 36 Pb 2 Ag

E = Eutectic

MP = Melting Point Only Estimated

\* = Difficult to solder because of high melting point

Alloys

#290. Has general characteristic of Indium (Indalloy #4) except that silver addition improves strength. Particularly useful for cryogenic applications.

#2. Especially useful for soldering against gold, as leaching is minimized. Has good thermal fatigue properties. Is compatible with Indalloys #204, #205, #7, #206, #10, and #150 in step-soldering applications.

#4. Good wettability on many surfaces, including ceramics, glass and quartz. Deform indefinitely under load so it has no tendency to embrittle, making it valuable for cryogenic applications.

#204, #205, #7, #206, #10, and #150. This group of lead-indium solders has been designed to cover the temperature range of 174°C-280°C. All have the minimum gold-leaching characteristics as well as the minimum gold-leaching properties of lead-indium alloys.

do not wet well, i.e., in the molten state they do not form a good cohesive bond with other metal surfaces, whether or not activating fluxes are used. Secondly, in general the lower the melting point, the lower the tensile strength of the solder. In addition, the presence of tin in the solder causes the molten solder bead to scavenge or leach gold from the plating of the metal contacts undergoing soldering. As the gold melts and becomes dissolved in the molten solder bead, its melting temperature increases, often by as much as 100°C, and its fracture toughness decreases.

It thus appeared that the best way to exploit a low temperature eutectic solder would be through the use of contact pads on the leadless chip carriers and on the logic panel which are not gold plated. This restriction presented a problem, since at the onset of the study, the commercially available leadless chip carriers used as the pad contact material 60 microinches of gold plating over 15 microinches of nickel alloy, both overlaid on an iron alloy for the pin body called Alloy 42. Discussions with the manufacturers of leadless chip carriers and dual in-line packages demonstrated that, if not gold plated in appropriate locations, the board surface and the chip carrier pads would oxidize rapidly; the components would thus have a shelf life of approximately six months unless stored in an inert gas atmosphere. A nongold material was required which could be plated on the leadless chip carrier

contact pads and would form a satisfactory bond to a low temperature, indium-based solder.

Several vendors of leadless chip carriers and dual in-line packages were queried regarding the availability of non-gold plating materials which would nonetheless retain good solder bonding properties. Kyoto Ceramics, Inc., the same company with whom the new leadless ceramic chip carriers are being developed, responded in the affirmative. Kyocera began experimenting in the fall of 1980 with a new plating alloy intended as a substitute for gold; this plating alloy, referred to as Kcillium, was reported by Kyocera to be a completely gold-free, nonoxidizing plating alloy, with good wetting properties assuming the use of conventional 60-40 tin-lead solder. The material content of this alloy was requested from Kyocera to allow an assessment of its compatibility with Indium/tin solders; however, the formula of this alloy is considered proprietary, and Kyocera refused to reveal its composition. Kyocera was willing to supply samples of dual in-line packages whose leads and attached lead frames had been plated with 15 microinches of nickel, followed by an overlayer of 30 microinches of the Kcillium alloy.

One of the components was subjected at Mayo to a mass spectrographic analysis of the outer 30 or 60 microinches of the surface plating, of the core of the lead frame, and of the 15 microinches below the Kcillium plating alloy. The mass

spectrographic analysis demonstrated alloy contents as depicted in Table 4; note that this first set of samples contained 10.3% (atomic percent) of gold, in contradistinction to the assertion by Kyocera of zero gold content. The results of this spectrographic analysis were supplied to Kyocera, along with a query regarding the presence of a nontrivial weight percent of gold. The remaining Kcillium plated dual in-line packages were subjected to a solder wetting tests using pencil irons, and a hot gas gun, and with wire solder and solder cream, as depicted in Table 3. This table also presents qualitative estimates of the ease of solder wetting of the Kcillium plating by the different solder formulations.

Based upon the mass spectrographic analysis of the first batch of Kcillium-plated parts, the materials engineers at the Kyoto Ceramics plant in Japan confirmed the high gold content, attributing this to contamination resulting from an incorrect manufacturing procedure. A second batch of components were then received, this time with a 60 microinch plating of Kcillium, which were again asserted to be free of gold. A mass spectrographic analysis indicated that the alloy constituency both in terms of the elements employed and their percentage composition by weight had changed considerably; nonetheless, a 1.8% residual gold content was detected. The results of solder wetting tests changed little, particularly given their qualitative nature, between the first and the second batches. However, the small residual gold content was still believed by Indium

TABLE 4

COMPOSITION OF ALLOYS EMPLOYED  
IN DUAL-IN-LINE PACKAGE PINS AND PLATING  
BY MASS SPECTROGRAPHIC ANALYSIS

Element and Spectral		Kcillium	
Line Examined	Alloy 42*	First Sample**	Second Sample°
Al KA	1.44	-----	----
Mn KA	.61	-----	----
Fe KA	71.72	2.15	.69
Co KA	.47	10.12	.29
Ni KA	22.29	29.24	2.15
Pd KA	3.48	48.16	94.52
Nb LA	-----	-----	.59
Au MA	-----	-----	1.76

\*All values stated in atomic percent

\*\*30 microinches Kcillium plated over 15 microinches nickel

°60 microinches Kcillium plated over 15 microinches nickel

Corporation of America to be sufficiently high to increase the melting temperature and lower the fracture toughness of a eutectic solder bead containing tin and Indium.

The results of the second set of tests were also reported to Kyocera, who replied that, due to a manufacturing problem, it will be very difficult to remove this last trace of gold contaminant. Kyoto Ceramics has now temporarily withdrawn Kcillium from consideration as a feasible plating alloy until the contamination problem is resolved. Conversely, they now suggest that, pending a resolution of the Kcillium contamination problem, reconsideration of gold plating on the chip carrier contacts is appropriate. Kyocera now offers two types of gold plating; the first, used for some time, plates 60 microinches of a rather porous layer of gold onto 15 microinches of a nickel underlayer; a newly introduced improved plating technique applies 15 microinches of an extremely nonporous gold to the same nickel underlayer. Because the 15 microinch layer is so dense, the total amount of gold per unit area is only slightly less than that in the 60 microinch layer. Nonetheless, the dense gold plating is somewhat more expensive.

As a result of the problems of gold leaching and subsequent solder bead fusion temperature increases and embrittlement if indium/tin-based low temperature eutectic solders are employed with gold-plated contacts, we have reluctantly set aside further consideration of eutectic solders until the

plating alloy problem is resolved. An additional difficulty in the use of eutectics is the difficulty of plating the contact pads of the circuit board with these alloys during its manufacture; none of the manufacturers of logic panels contacted is able to plate large areas with other than tin or conventional tin-lead solder. This problem could almost certainly be circumvented by a "preplating" step using eutectic solder cream reflowed onto the contacts in a vapor phase solder reflow machine. Hence, provided that the gold plating on the chip carrier contacts can eventually be replaced with a gold-free alloy, consideration of eutectic solders will be reopened; exotic eutectic alloy solders would allow lower soldering temperatures, easier removal of components during rework, and higher solder bead malleability, though at the loss of some breaking strength.

#### 4. Soldering Methods

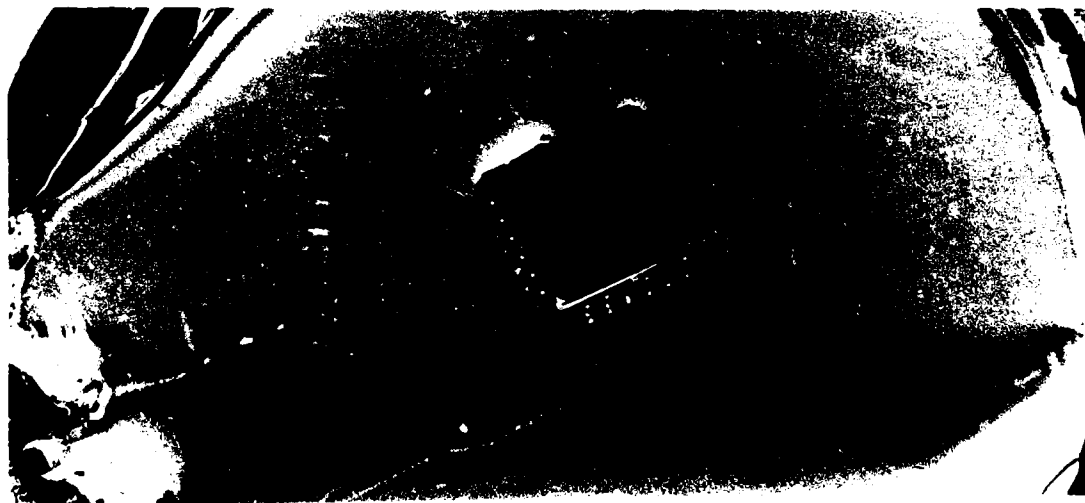
Four basic methods have been investigated at Mayo for the solder attachment of leadless chip carriers, chip capacitors, and terminator packs to the logic boards described earlier, most of which have several variants. Potentially useful soldering methods fall into two categories, that of 1) manual bonding of individual components to the board, either during a rework cycle or for initial installation; and 2) mass bonding, whereby all or most components are soldered to the board in a single operation. The traditional soldering pencil widely used for hand

installation of leaded flat packs was found suitable in tests conducted here (see below) for manual bonding of leadless chip carriers to a variety of test circuit boards with and without wire wrap pins. The solder should be pretinned onto the leadless chip carriers and boards prior to component installation, requiring thereafter only a small amount of activating flux or solder cream to be added during the attachment operation. Pretinning of logic boards with 60-40 tin-lead solder is a standard procedure, and was tested in the studies described below.

Pretinning of the leadless chip carrier pads may be performed either manually or, as tested successfully here, by prewarming the leadless chip carriers in a small oven or hot plate, and then by "floating" the leadless chip carriers on a pool of molten metal in a small solder pot; as depicted in Figure 50, this tinning method is nearly instantaneous, appears not to damage the leadless chip carriers, and creates a uniform tinning of flush contact pads or the tungsten mounting bumps depicted in Figures 27 and 28. The solder can also be applied in wire form with or without a flux core, but this is a much more tedious operation than direct plating onto the board and solder pot tinning ("float tinning") of the leadless chip carriers. Solder can also be applied to the mating surfaces of the chip carrier and board in the form of a "cream" consisting of finely divided particles of solder uniformly distributed by a ball milling process into a flux base; the

individual particles of solder do not exceed 200 mesh diameter. Several techniques are available to apply the solder cream to the mating surfaces, as will be described later.

In addition to the use of soldering pencils for manual attachment of the leadless chip carriers and other components to the logic boards, a handheld hot gas gun approach was also found suitable. Two models of such hot gas guns were purchased and tested. The more elegant unit tested, a Model FA068 manufactured by Edsyn Corporation, appeared not to deliver sufficient thermal output for reliable solder bonding. Conversely, the less expensive unit, a Model T-100-1, manufactured by



LEADLESS CERAMIC CHIP CARRIER FLOATING ON SOLDER POT

Figure 50

EJ & F Engineering Corporation, has proven to be satisfactory for hand soldering of small components without direct contact of the solder tool with the workpiece, delivering sufficient thermal energy to a localized area to fuse single contacts rapidly. Both direct contact pencil soldering elements and hot gas soldering tools of the type manufactured by EJ & F Engineering Corporation must be available for rapid repair and rework of previously fabricated logic panels, and can be also used for all component bonding of a board when necessary, although this procedure is quite tedious. In conjunction with these hand tools, a PAK-X-TRAC Model PXT-44A-DM chip carrier removal tool, manufactured by Nu Concept Computer Systems, has also been tested. This simple hand held device heats the edges of the chip carrier simultaneously and uniformly, thereby allowing a liftoff of the chip carrier without destruction of the underlying traces on the logic board; this unit will be described later.

The second class of solder bonding methods are those designed for mass attachment of multiple components to the board in a single operation. Four methods have been reviewed, only one of which has undergone serious operational testing: 1) infrared soldering; 2) oven-based hot gas convection soldering; 3) wave soldering; and 4) vapor phase reflow soldering. Wave soldering was rejected very early in the study, as it is oriented toward relatively large production runs and is unsuitable for use in a prototype laboratory environment. Since

wave solder machines employ large pool of molten solder, the surface of which is blown into a "wave" by air pressure, the approach is not adaptable to the use of exotic solders whose cost per pound is relatively high. In addition, components must be mounted securely, usually with pins protruding through plated through holes in a logic panel; as the bottom of the board is passed through the wave, molten metal is wicked up through the holes. Wave soldering of surface mounted components which are not physically held in position is difficult. Wave soldering is, therefore, best suited to mechanically inserted components such as dual in-line packages, leaded resistors, and capacitors, etc., but not to structures such as chip capacitors, leadless chip carriers, and surface mount chip carrier connectors. In addition, the large contact area of the solder pool with the board undergoing soldering requires relatively large metal-free guard bands between conductors and contacts to prevent the formation of solder bridges which create short circuits, thereby necessitating rework operations.

Three additional methods were compared and contrasted with one another in a single review process. Dry gas convection soldering (essentially a larger version of the manual hot gas gun described earlier), and infrared soldering were first examined, because of their conceptual simplicity and because these techniques are used in other Mayo laboratories for a variety of chemical activation and drydown procedures. These two techniques have the advantage of widespread use over many

years, and are thoroughly understood. The equipment for these soldering procedures is readily available, and the methods themselves are quite suitable for fabricating a small number of logic panels in a prototype laboratory environment. However, because of the relatively slow heat transfer to the boards in the dry gas technique, and the relatively long "heat soak" duration of the infrared process, a prolonged exposure of the board and components to the high temperature environment is required. Further, unless an inert gas is used in conjunction with these processes, some high temperature oxidation of the plating surfaces must be expected, thereby increasing contamination of the solder joints and possible oxygen embrittlement of the solder beads.

By contrast, the technique of vapor phase reflow soldering, jointly pioneered by Western Electric Corporation, Minnesota Mining and Manufacturing, Inc., and Hybrid Technology Corporation, is a completely new approach to high-speed oxidation-free soldering, which in effect selectively delivers heat directly to the surface areas of the parts undergoing bonding. Although the details of the vapor phase reflow technique will be presented later in this report, the basic principle is quite straightforward. An inert liquid, a fluorine-substituted long-chain hydrocarbon with a boiling point 20-30 degrees Fahrenheit above the fusion temperature of the solder, is boiled in a closed container, creating a vapor cloud above and in thermal equilibrium with the liquid.

In a refinement of this procedure, an insulating blanket of another inert gas such as freon TF is layered above the denser blanket of fluorocarbon vapor.

If a logic board with prepositioned pretinned components is lowered through the Freon TF blanket into the fluorocarbon vapor cloud, the vapor rapidly condenses on all exposed surfaces, rapidly transferring its latent heat of condensation (its latent heat of vaporization) of 16 calories/gram to the component surfaces. Since the heat of vaporization of a liquid per unit weight is much higher than the heat capacity per degree Centigrade of the material in gaseous or liquid form, an extremely rapid heat transfer to the surfaces undergoing soldering at constant temperature is achieved. For example, depending upon the materials being soldered and the size of the reflow machine, even very large boards can be completely soldered in 15-30 seconds.

Such short soldering durations minimize heat soaking of the board and components: although the surfaces of the board rapidly reach the solder fusion temperature, the cores of the boards and components may not achieve the full solder temperature. The condensed liquid streams from the board surfaces, providing a minimal flux cleaning action. Since the fluorocarbon vapor is inert and completely blankets the board, oxidation does not occur. The now soldered board is raised into

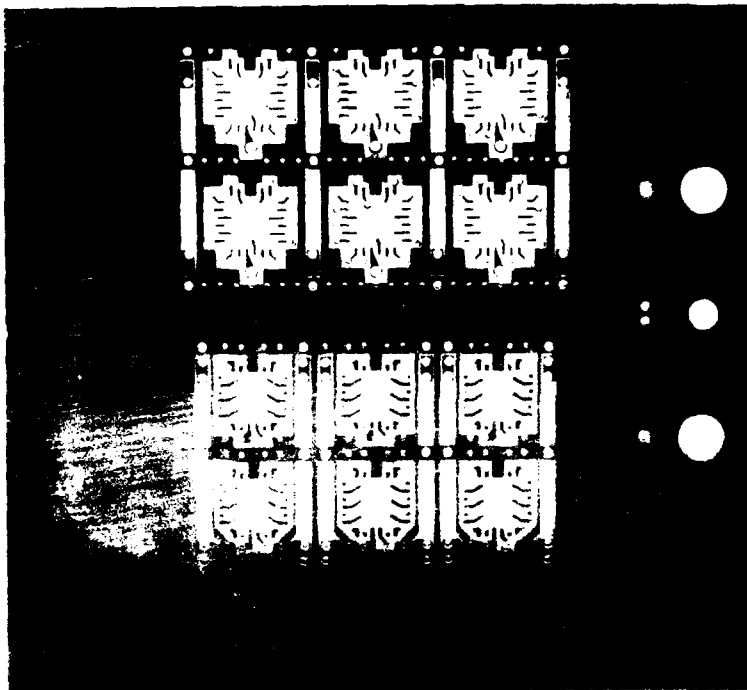
the freon gas blanket, which is maintained at a lower temperature than the fluorocarbon gas; cooling thus begins while the board remains in an inert gas environment. The board emerges from the machine partially cooled and only slightly above the solder fusion temperature. Vapor phase reflow machines are suitable for mass production or for single board runs, and are thus ideal for a wide range of production environments including system prototype laboratories.

Because of the apparent match to the system prototyping capabilities under development in this project, and the short thermal exposures which place minimum stress on delicate components, our review concentrated on vapor phase reflow for mass component attachment, and conventional soldering pencils and hot gas guns for individual component installation. It should be noted that a hot gas solder pencil almost certainly could be modified to use a stream of gaseous fluorocarbon rather than superheated air, with the heat transfer via the latent heat of condensation of the fluorocarbon; however, the toxicity of the fluorocarbon liquid would require the use of such a hot gas gun within a vented chemical hood, and the loss of gaseous fluorocarbon would be both expensive (\$600/gallon) and environmentally hazardous.

##### 5. Prototype Board Fabrication and Solder Tests

In order to test a variety of solder bonding methods, special solders, and board fabrication techniques, prototype

printed circuit boards consisting of one, two, or three separate layers were fabricated in several different styles. Figure 51 shows the component side of one of these logic panels. Each of the twelve patterns, or subarrays, on the board was optimized for a 24-pin leadless chip carrier manufactured in different versions by Kyoto Ceramics and 3M Corporation; the foil trace widths in the upper six circuit patterns are 20 mils wide, while the lower six patterns employ 30 mil traces. The vertical columnar patterns between the chip carriers allowed the installation of the single-in-line package ECL terminators described in the Year 1 Interim Report. The boards were drilled to accommodate the headless wire wrap



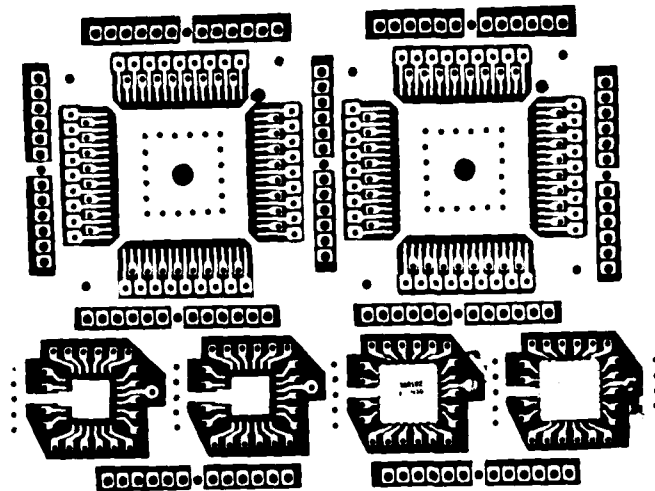
LEADLESS CHIP CARRIER SOLDER TEST BOARD

Figure 51

pins developed by Augat, Inc., and described earlier. In addition to the layer depicted in Figure 51, two pattern layers were modified for use as -2 volt and -4.5 volt busses when full operation of the circuit was contemplated. In addition, several boards were fabricated with patterns for both the 24-pin and the 68-pin JEDEC Type A leadless ceramic chip carriers.

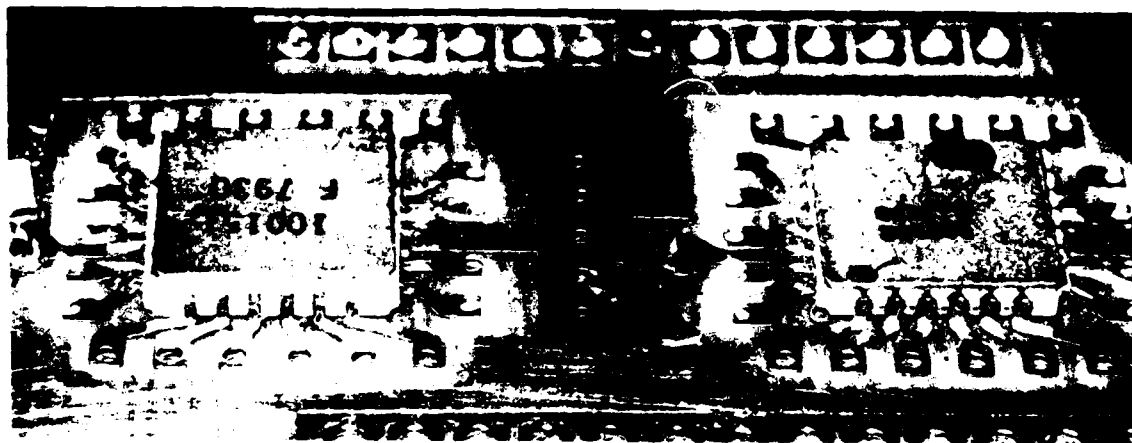
One of the most critical questions regarding fabrication was the optimum method of applying conventional or indium-based eutectic solders to the board surfaces and leadless chip carrier contacts. In the initial studies, either the pretinning of the chip carriers by the "float" process, or the application of solder cream to the chip carrier contact pads appeared equally feasible. As testing proceeded, it became clear that either method would suffice for manual solder bonding, but both approaches were required for vapor phase reflow soldering; in the latter case, the tinning of the chip carriers provides sufficient solder at the appropriate location, while the use of solder cream temporarily "glues" the carriers in position and provides the small amount of flux necessary to insure a uniform reflow of the solder bead.

Figures 51 and 52 depict the first of six separate sets of tests; this first experiment was performed with a single layer board containing patterns for 24-pad and 68-pad leadless ceramic chip carriers. The board was pretinned with



SOLDER TEST BOARD PREPLATED WITH 3 MILS OF 60/40 TIN-LEAD SOLDER

Figure 52



LEADLESS CHIP CARRIERS SOLDERED IN PLACE WITH SOLDERING PENCIL

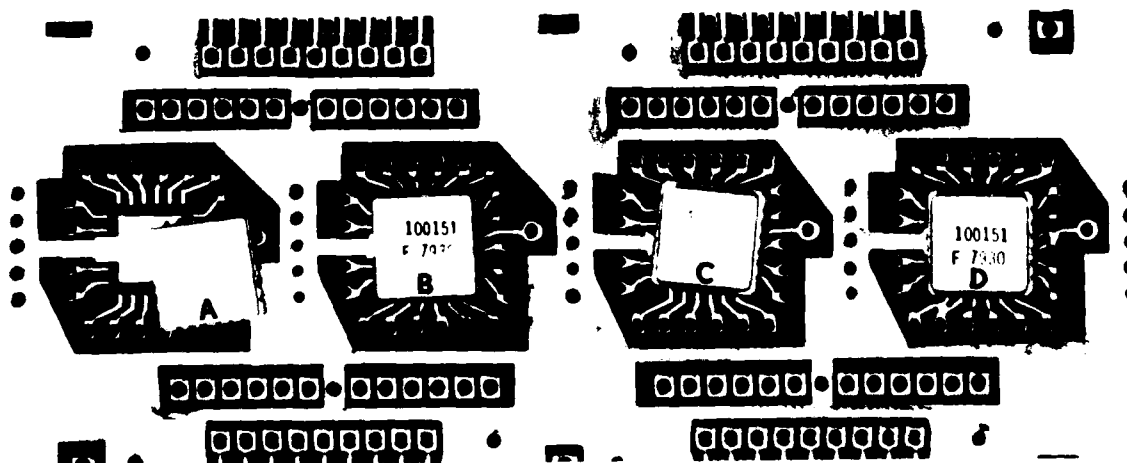
Figure 53

3 mils of 60-40 tin-lead solder; two ceramic leadless chip carriers were manually solder bonded with a soldering pencil using neither flux nor solder paste. The leadless chip carriers were first float tinned; the solder pencil was then used to reflow the plated solder on the board surface to the contact pads on the chip carriers. Figure 53 also depicts a small chip capacitor attached in a similar matter. This first test provided a performance baseline using proven mechanical bonding tools and techniques to serve as the reference for later solder bonding studies with alternate techniques.

An overview of the results of the second experiment, using alternate bonding techniques, is depicted in Figure 54. Figure 56 depicts the rightmost two chip carriers of Figure 54, while Figure 55 depicts the leftmost two carriers. Each of these components was pretreated by a different technique, followed by positioning of all four chip carriers on a test board pretinned with 3 mils of 60-40 tin-lead solder. The board was then soldered in a Hybrid Technology Corporation vapor phase reflow machine the use of which was donated by 3M Corporation of Minneapolis. Note the mottled, wavy appearance of the board surface in Figure 54, which is even more apparent when the boards are viewed with the naked eye. The vapor phase reflow technique is not compatible with the deposition of more than .5 mil of solder by preplating of the boards. A thick layer of preplated solder becomes a molten pool which, with the assistance of the condensing fluorocarbon liquid pouring from the

board, acts as a liquid bearing to float the chip carriers completely out of alignment. When the board is removed from the vapor phase reflow machine, the components "freeze" to the board completely out of alignment with their intended position.

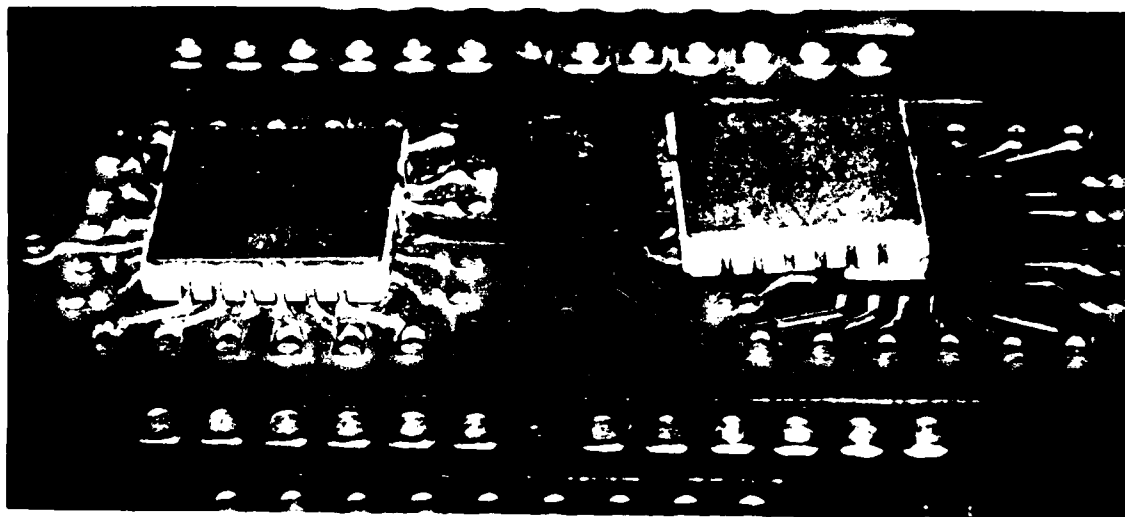
The chip carrier labeled "A" in Figure 55 was pretinned by the "float" technique, a small amount of flux was applied to each pretinned pad, the chip was placed on the logic panel, and the high volatility solvents were removed from the flux with a hot air gun. The flux thus functioned as a low strength



VAPOR PHASE REFLOW SOLDER TEST BOARD PREPLATED  
WITH 3 MILS OF SOLDER. EACH CHIP CARRIER  
PRETREATED BY A DIFFERENT METHOD.

Figure 54

adhesive to maintain the chip carrier in position through the early stages of the vapor phase reflow operation. The carrier labeled "B" in Figure 55 was also pretinned by the float process, followed by the application of a small amount of Dupont 4499 solder cream to the contact pads on the logic board. After positioning of the chip carrier on the board pattern, the solder cream solvent was driven off as described above. Note that the Dupont 4499 solder cream paste was applied as a continuous thin bead completely around the perimeter of the chip carrier pattern on the board, with no attempt to subdivide the bead into small droplets confined only to the contact pads. This test was performed to ascertain if the application of solder cream in a continuous bead would result in short circuiting of the individual contacts one to another,

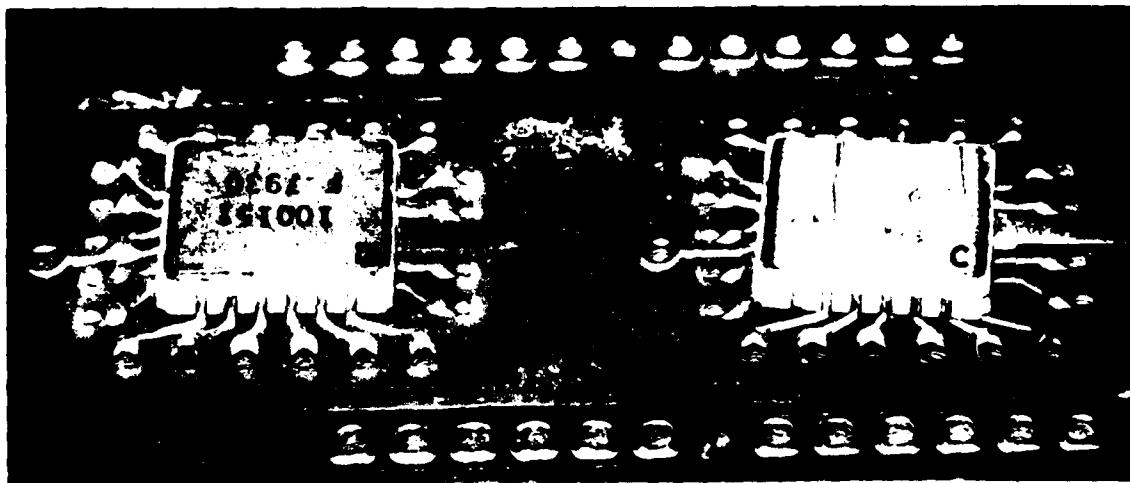


CLOSEUP VIEW OF TWO LEFTMOST  
COMPONENTS IN FIGURE 54.

Figure 55

or whether cohesive forces within the molten solder would automatically subdivide the bead into droplets colocated with the board contact pads.

The leadless chip carrier labeled "C" in Figure 56 was also float tinned; a small amount of solder cream was applied to the center of the chip carrier pattern to hold the chip in position; a small amount of solder-free flux was then applied to the logic board directly under the edge of the chip carrier to activate the solder beads. The chip carrier labeled "D" in Figure 56 was also float tinned, with only solder cream applied to the perimeter of the chip carrier footprint on the board well beyond the edges of the chip carrier. Note that only the chip carrier labeled "D" remained in position; all

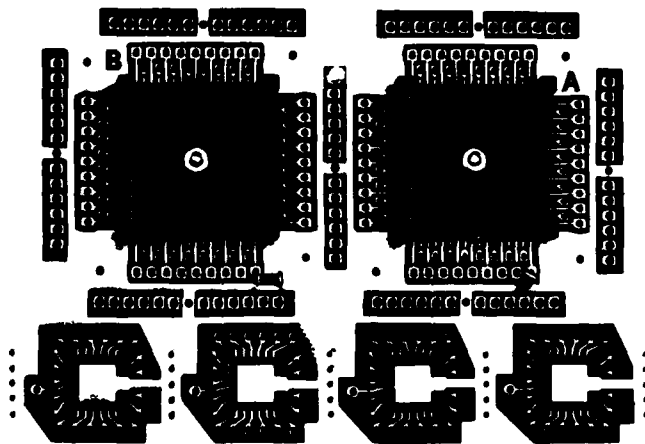


CLOSEUP VIEW OF RIGHTMOST TWO  
COMPONENTS OF FIGURE 54.

Figure 56

other chip carriers moved out of position to some degree, particularly chip carrier "A" which floated completely off the contact pad. This test clearly demonstrated that vapor phase reflow requires very precise control of the amount and placement of solder applied to the substrate board.

Figures 57, 58, and 48 display the results of a third solder test performed with 68-pin leadless chip carrier connectors manufactured by Augat, Inc. Both components were soldered to the board using vapor phase reflow, as were the two small chip capacitors visible in Figure 58. The leadless chip carrier connector labeled "A" in Figure 58 was pretinned by a modified float process; socket "B" was not pretinned. Along one edge of each 68-pin board pattern a thin stripe of

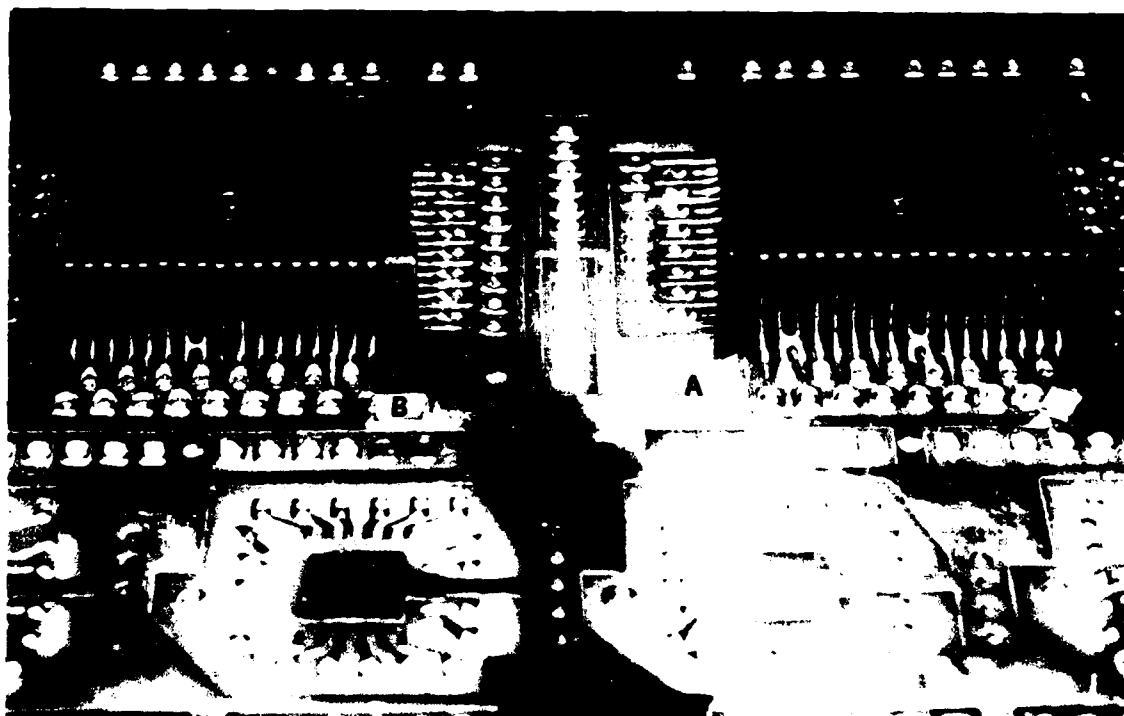


VAPOR PHASE REFLOW BONDING OF LEADLESS CHIP  
CARRIER CONNECTORS TO SOLDER TEST BOARDS.

Figure 57

Dupont 4499 solder cream (composition - 36% lead, 62% tin, and 2% silver) was applied; the other three edges of both board patterns were left untreated. Figure 58 is a photomicrograph of the edges of the two chip carrier connectors on which the stripe of solder cream had been applied prior to vapor phase reflow. In both cases, several pin-to-pin solder bridges are visible.

Figure 48 is a photomicrograph of the opposite sides of the two connectors, where no solder cream had been applied.



CLOSEUP VIEW OF 68-PAD LEADLESS CHIP CARRIER CONNECTORS  
VAPOR PHASE REFLOW SOLDERED TO TEST BOARD

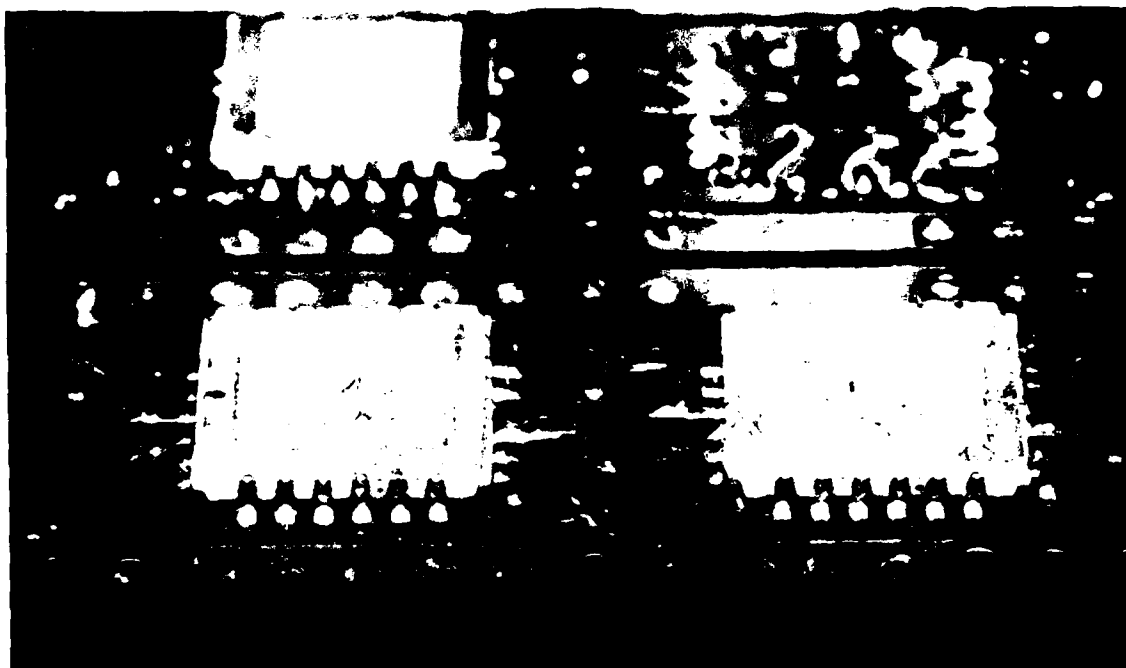
Figure 58

Although connector "A" had been pretinned but connector "B" had not, it is clear that 3 mil layer of plated solder on the board provided sufficient metal to create near perfect bonds for all contacts on both connectors. However, as demonstrated in the prior test, the thick solder plating can provide such a large excess of molten metal that chip carriers, if not the connectors, are moved out of position during the reflow operation.

The fourth set of solder tests was performed on a board, containing twelve patterns for 24-pin leadless chip carriers, which had been preplated with .25-1 mil of standard tin plating (i.e., not solder) to allow assessment of the effects of local application of solder cream alone. The components labeled A were assembled by manually solder plating the contact pads on the logic board and hand soldering the float tinned chip carriers to the board with a pencil (Figure 59). All four components were soldered in the same manner, after which the two chip carrier patterns closest to the upper edge of the photo were then subjected to component removal tests using a leadless chip carrier solder removal tool manufactured by Nu-Concept Computer Systems, to be described later. Figure 60 depicts two leadless chip carriers pretinned by the float process, and then manually soldered; the board patterns were not manually pretinned with solder prior to the emplacement of the chip carriers. Comparison of Figures 59 and 60 indicate that the prior application of a very minimal amount of solder to the

board pattern results in a much cleaner final result, since excess solder is heavily wicked into the chip carrier edge castellations, creating nonuniform solder bonds.

Figure 61 depicts two styles of leadless chip carrier vapor phase reflow solder bonded to the logic panel prior to their removal by the PAK-X-TRAC Model PXT-44A-LM chip carrier removal tool. Figure 62 is a photomicrograph of two of these patterns following removal of the components with the chip carrier removal tool. Although the amount of solder remaining



LEADLESS CHIP CARRIERS HAND SOLDERED TO TEST  
BOARD AFTER HAND TINNING OF BOARD CONTACTS

Figure 59

on the boards was excessive (these two patterns were the ones heavily pretinned with solder prior to the bonding operation), all but one of the foil traces is intact (the second from rightmost trace along the lower edge of the righthand pattern is missing). Though the traces would have to be cleaned and solder wicked before reinstallation of a component, these early tests indicate that a component removal and replacement operation is feasible.



LEADLESS CHIP CARRIERS HAND SOLDERED TO  
TEST BOARD WITHOUT PRIOR TINNING OF BOARD PATTERNS

Figure 60

Figure 63 depicts an overview of a 12 pattern board in which numerous chip carrier and board pretreatment methods were validated simultaneously; all components were solder bonded simultaneously using vapor phase reflow. The board was plated with .5-1.0 mils of tin; all solder was supplied by the prior application of the alloy to the chip carriers and the board contact pads using a variety of methods. The chip carriers labeled "A" in Figure 63 were pretinned by the float process, but no additional solder cream was added; a small amount of flux was applied at two corners of each chip carrier to maintain their positions during the vapor phase reflow. The chip carriers labeled "B" in Figure 63 were pretinned by the float process; a small amount of solder cream was applied to each of the chip carrier contact pads. The chip carriers were then placed on the board, and the volatile solvents in the solder cream were evaporated.



COMPONENTS ATTACHED TO CIRCUIT BOARD  
BY VAPOR PHASE REFLOW PROCESS

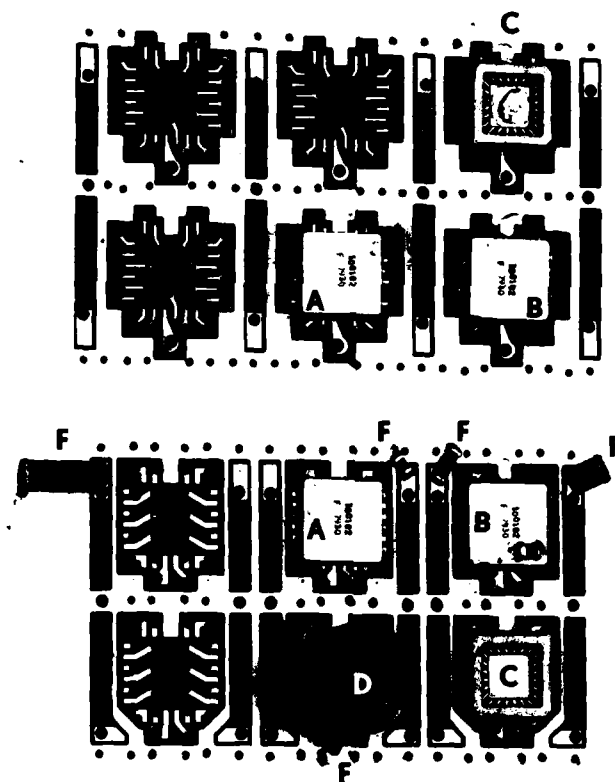
Figure 61



PHOTOMICROGRAPH OF SOLDER TEST  
BOARD SURFACE AFTER REMOVAL OF LEADLESS  
CHIP CARRIERS WITH REMOVAL TOOL.

Figure 62

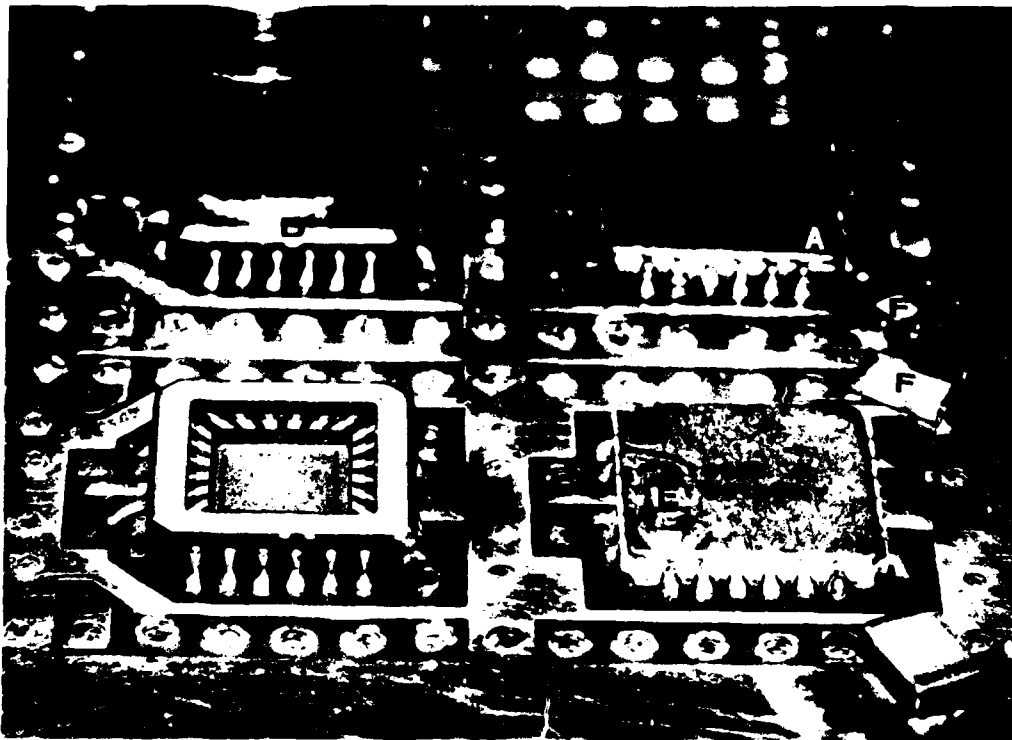
The chip carriers labeled "C" in Figure 63 were test parts specially fabricated with 5 mil tungsten bumps as their electrical contacts. These chip carriers were pretinned by "floating", followed by manual application of Dupont 4499 solder cream to the tinned bumps. For the chip carriers labeled D, a milled copper heat stud was positioned on the lid surface of the chip carrier, with a thin layer of solder cream applied to the interface between the lid and the bottom



SOLDER TEST BOARD WITH MULTIPLE LEADLESS  
CHIP CARRIERS BONDED BY DIFFERENT TECHNIQUES

Figure 63

of the stud. Figure 64 is a photomicrograph of components A, B, C, and D, depicting the attachment of the stud to the chip carrier lid. Although the stud moved slightly during reflow, it is thermally and mechanically bonded to the lid. The prototype chip carrier with the 5 mil tungsten bumps also reflowed properly. Vapor phase reflow attachment of small decoupling chip capacitors to the Kovar lid of the chip carrier demonstrates that bonding of decoupling capacitors to the ceramic back of the Mayo-designed leadless chip carrier of Figures 25 and 26 will also be feasible. Note also that

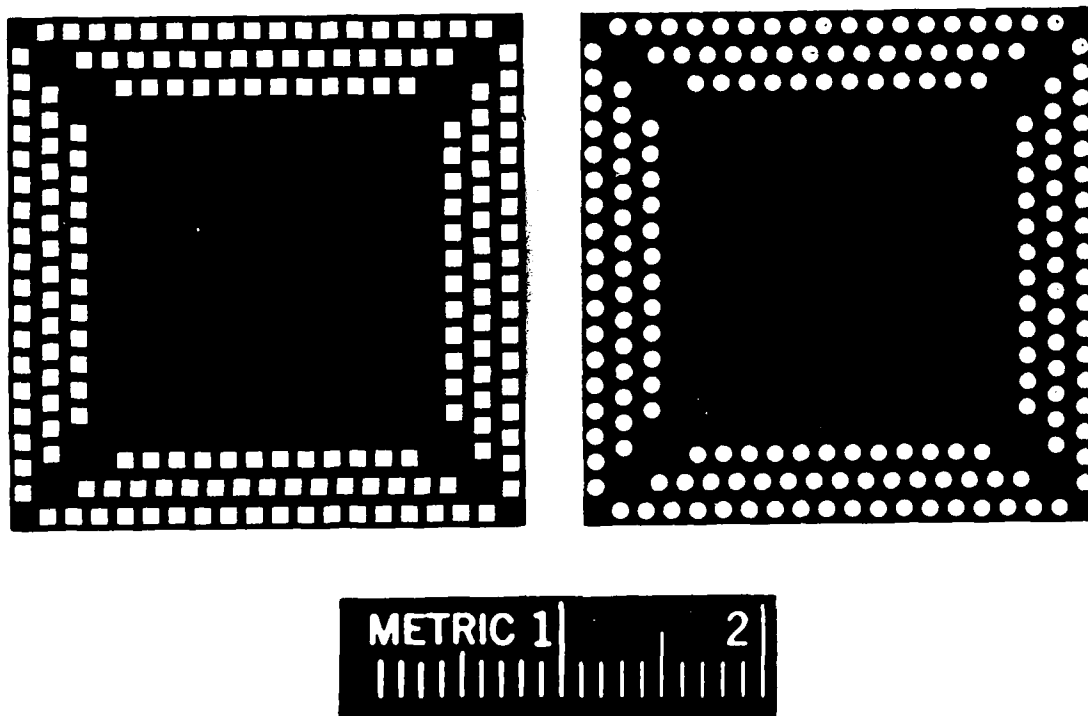


PHOTOMICROGRAPH OF SEVERAL COMPONENTS  
SHOWN IN FIGURE 63

Figure 64

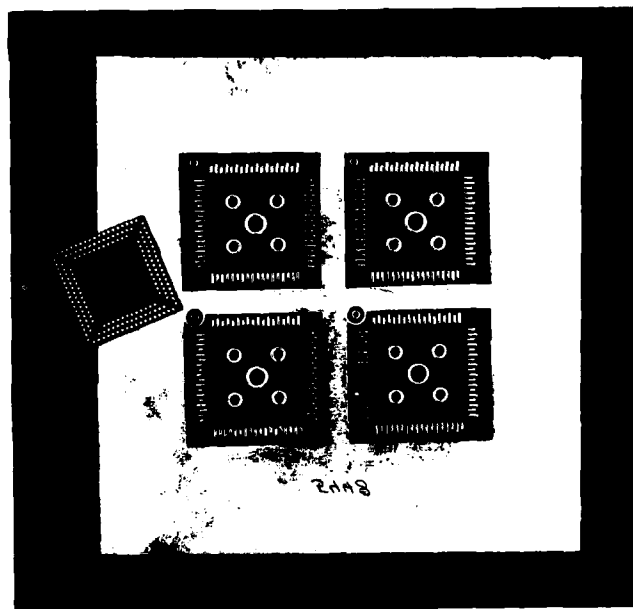
larger chip capacitors were also reflow attached to the board in the same operation.

Lastly, Figures 65 and 66 depict a new 180-pad, triple row solder test blank and an appropriate solder test board with plated through holes, which will allow testing of the feasibility of vapor phase reflow solder bonding large leadless chip carriers with two or three concentric rows of



SOLDER TEST BLANKS FOR  
180-PAD LEADLESS CHIP CARRIER

Figure 65



SOLDER TEST BOARD FOR EXPERIMENTAL  
180-PAD LEADLESS CERAMIC CHIP CARRIER.  
PLATED VIAS ALLOW INTEGRITY TESTING OF  
INNER SOLDER BONDS

Figure 66

contact pins. Although it is feasible to fabricate a chip carrier and a matching logic board for such a padout footprint, it is not clear that the inner rows of contact pads can be successfully soldered; it may be difficult for the fluorocarbon gas to reach and rapidly heat the inner rows of contacts. The test board and the 180 pad test blanks were not fabricated in time to undergo vapor phase reflow tests for the Year 2 effort, but will be studied during the first quarter of Year 3. The entire question of optimum board design and fabrication techniques for chip carriers requiring so many padouts is in doubt at the present, and will be examined during the coming year.

In summary of the results of these solder tests, the best approaches for small leadless ceramic chip carriers are now clear. The best electrical contact and the easiest board cleaning after soldering can be achieved with the tungsten "bumped" leadless chip carriers; manual soldering of bumped chip carriers to a board is by means of fillet joints to the edge castellations, whereas the vapor phase approach reflows solder between the board and the bottoms of the bumps. For the vapor phase reflow process, the leadless chip carriers should be pretinned, preferably by the float process, and a small amount of solder cream applied to the chip carrier or the logic panel contacts to assure a good reflow bond. Preplating of more than a very thin layer of solder onto the logic panel is generally unsatisfactory and largely unnecessary;

the more selective application of solder cream appears to be optimum. The application of flux rather than solder cream is feasible, but is not as reliable as solder cream. Lastly, vapor phase reflow bonding for mass attachment of components is straightforward and yields good quality bonds, provided that care is taken in the preparation steps, as described above.

#### 6. Application of Solder Creams by Silk-Screening or Pressure Dispensers

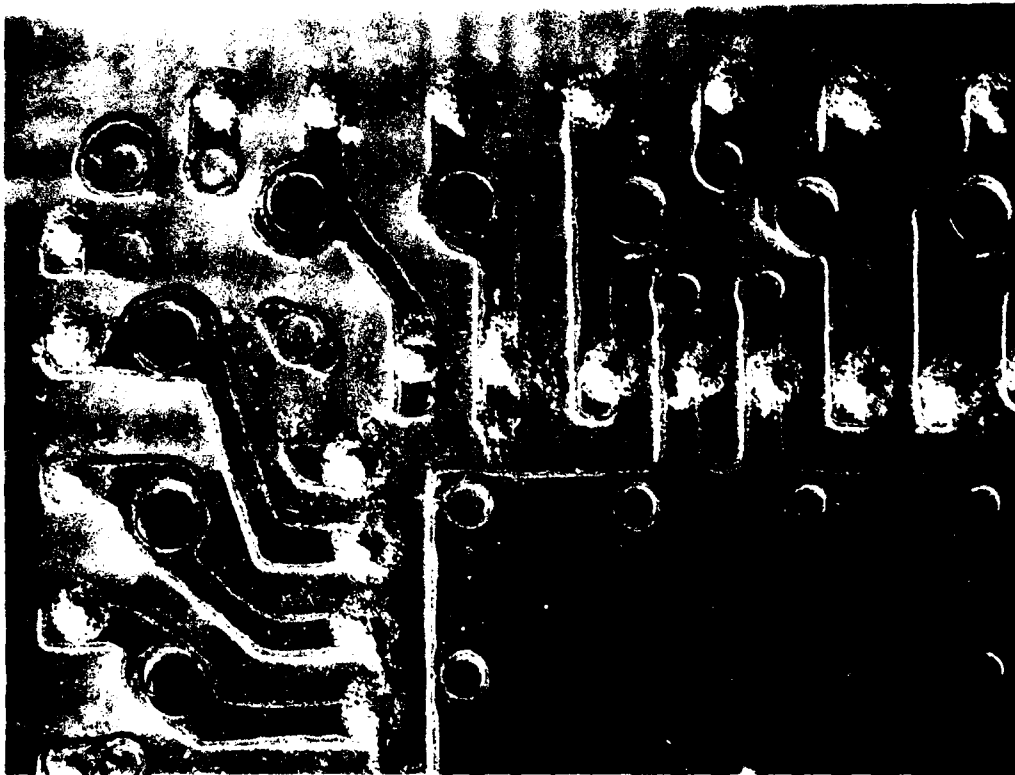
The mechanism by which solder cream is applied to the components or to the circuit board patterns is critical, particularly for vapor phase reflow, since insufficient solder cream application results in bonding failure, whereas excessive application of material creates solder bridges between adjacent conductors. As a result of the sensitivity of this step, three mechanisms have been investigated for applying solder paste to the leadless chip carriers or to the logic panels, two of which have been tested in this laboratory. The first approach, widely employed in mass production manufacturing, is the fabrication of a silk screen mask for the entire logic board, and application of the solder paste through the silk screen. Discussions with vendors and manufacturers of silk screens and screening equipment highlighted the difficulty of this approach in a laboratory prototyping environment. The silk screen method is unsuited to production runs of only a

few boards of a given design, since the alignment procedures are complex, considerable skill is needed in the application of the solder cream to the screened board, and a change in board style requires the manufacture of a new silk screen. Further, this process requires the logic boards to have no protrusions on the surface to be screened, since the screen is deformed over a region far beyond the protrusion itself. Since in a prototyping environment specialized logic boards may have connectors, special sockets, etc., installed on the board during manufacture, a truly flat board surface cannot be guaranteed.

It appeared possible to apply the solder cream to the contact pads on the chip carriers, particularly those fabricated with tungsten bumps, by milling an aluminum cylindrical roller much like a printer's ink spreader, and spreading the solder cream on an optically flat glass surface to a calibrated thickness. The chip carriers were then gently touched to the cream-covered surface. Although several thicknesses of cream were attempted (5 mils, 10 mils, and 20 mils), this method proved to be unreliable.

The third method attempted has been successful in all tests to the present, and appears promising for the application of solder cream to localized areas of a logic panel in a system prototype environment. Several companies, including

Tridak Corporation, manufacture specialized machines for dispensing small, measured quantities under controlled air pressure of highly viscous liquids, including solder creams and paste fluxes. A Tridak Model 200V viscous liquid dispenser was purchased; only a small amount of experimentation was required to perfect a manual method for dispensing small uniform quantities of solder cream onto the contact pads of the logic board. Although the Tridak Model 200V is a manual machine, the vendor also manufactures a larger unit, Model 280J, which can dispense the solder cream through a multiorifice manifold onto an entire chip carrier subarray pattern on a logic board in a single operation. Figure 67 is a photomicrograph of the deposition of small amounts of solder cream onto the contact pads of a test board using the manually operated dispenser; although only a single bolus of solder cream was applied at a time, less than a minute was required to "dispense" the entire set of patterns visible in the photograph. Further investigation of these types of pressurized viscous liquid dispensers will be performed in the first quarter of Year 3.



PHOTOMICROGRAPH OF SOLDER TEST BOARD  
WITH DOTS OF SOLDER CREAM APPLIED WITH  
PNEUMATIC PRESSURIZED APPLICATOR.

Figure 67

## SECTION VII

### DESIGN OF HIGH FREQUENCY TERMINATOR PACKS FOR USE WITH LEADLESS CERAMIC CHIP CARRIERS

In a transmission line interconnect environment, terminations must be provided for each of the active signal strings on the logic board; the selection of the appropriate one of several different types of transmission line protocols is dependent upon the specific application. For example, as described in the Year 1 Interim Report, the use of a mixture of single-ended and differential protocols in the same multipanel system allows optimization of the protocol to the particular need. On a single logic panel, for example, data strings can be treated as single rail (one signal line sandwiched between A.C. ground planes, or one signal wire twisted with one ground wire) transmission lines, with a termination to the reference voltage through a resistor whose value equals the average impedance of the transmission line. This so-called "shunt terminated" protocol is the most convenient because it requires only a single terminator resistor at the last destination node of the signal string, is reasonably immune to noise if the signal string remains on a single logic panel, and exhibits the most rapid rise and fall times of all protocols employed (see Year 1 Interim Report, pages 31-46). Conversely, for signals transmitted between logic panels, the Year 1 Interim Report demonstrated that the use of a differential transmission

line protocol, with both true and complement signals transmitted between boards, yields by far the highest noise immunity and the maximum possible data transmission rate per signal.

These two protocols (as described in the Year 1 Report, there are many other self consistent sets of protocols for special cases), require a total of three types of resistor terminator networks. One type of terminator network for the shunt protocol contains multiple resistors each connected at one end to the individual signal strings and, at the other end, to a bus inside the terminator pack which is in turn tied to the logic LOW reference voltage (-2 volts for ECL). For the differential transmission protocol, two types of terminator packs are required. One type contains isolated resistors, each of which is connected between the true and complement signal lines at the last destination in the string. The second type contains so-called "pull-down" resistors, two of which must be connected between the true side and complement side of the source driver gates and the largest negative voltage in the system, which, for subnanosecond ECL, is -4.5 volts (see the Figure on page 34 of the Year 1 Interim Report).

These termination and pull-down resistors may be incorporate directly into a logic board by creating a buried layer plane containing a large number of thick film deposited resistors, connected to the last node in each signal string through

a "via" interconnection. The resistors in the terminator plane must be committed to the signal strings at the time of board manufacture; it is extremely difficult to fabricate the board and commit the buried resistors thereafter. Unfortunately, the ability to commit the terminators after board fabrication is exactly the capability required in a system prototyping environment; that is, it is desirable to be able to manufacture universal logic boards, with final circuits laid out on the board by backplane wiring only as necessary. Hence, although terminator pack resistors require more logic board area than would the buried layer resistors, they appear to be the only acceptable approach for a universal logic board. Two or at most three different designs for pack terminators are sufficient to allow several of the available transmission line termination protocols to be exploited: shunt terminated transmission for all data and most clock signals confined to a single logic panel, differential or dual single rail transmission of clock signals on large logic panels, and fully differential signal transmission for both data and clock signals between logic panels.

This versatility was exploited by the specially designed ECL terminator packs described in the Year 1 Interim Report; for similar reasons the new logic board and fabrication protocols for leadless chip carriers will also exploit high density terminator packs, redesigned for the new boards and, it is

hoped, with improved electrical performance. The design constraints for these new terminators will be described in the following paragraphs.

It was expected that the new pack terminators would be fabricated using small 94% alumina ceramic blanks, with deposited thick film resistors interconnected with plated metal traces (see pages 19-27 of Year 1 Interim Report). Based upon the prior experience gained in the Year 1 effort, it appeared feasible to design pack terminators whose electrical performance would exceed that of the Year 1 designs. A fundamental design decision was required concerning the inclusion in the new designs of socket pins (see Figure 7, page 20, Year 1 Report), or deletion of the pins and reliance only on solder contact pads similar to those of the leadless chip carriers. If pins were used, matching pin sockets in a single in-line configuration would also be required on the logic board; undoubtedly the Y-shaped terminator pins and the board socket pins would contribute to increases in shunt capacitance and series inductance and degrade the high frequency performance of the terminators. Hence, the use of contact pads rather than pins appeared to be the better electrical design approach.

Conversely, the use of contact pads rather than pins appeared likely to cause board assembly problems, since without pins it would be difficult to install the terminators and make electrical contact with the individual resistors in the pack. The design which evolved employs a pair of pins, one

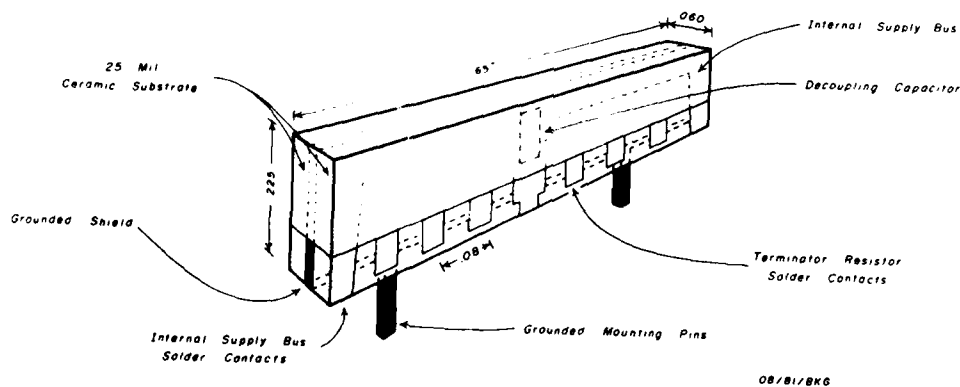
at each end of the terminator, for mechanical insertion, but not to support electrical contact between the logic strings and the pack resistors. In the most recent design, this philosophy has been violated somewhat; the two positioning pins also connect a buried ground plane within the terminator pack to the logic board ground plane, as will be described below.

Because the achievement of maximal resistor density in the terminator packs was of paramount importance, the possibility of depositing resistors on both sides of the ceramic substrate was investigated. Discarding the use of conventional pins (as were employed in the design of terminator packs for the DIP boards described in the Year 1 Report), which must be supported on both sides of the ceramic substrate, would indeed allow the deposition of thick film resistors on both sides. A review of possible manufacturing approaches indicated that double sided terminator packs could be fabricated as a pair of thin ceramic substrates, each with resistors deposited on one side, followed by back-to-back bonding of the two ceramic blanks. In a last step, ceramic conformal coating would be applied to the completed structure.

This fabrication approach made it feasible to add an additional electrical performance feature to the design. Rather than bonding the bare ceramic surfaces together with a nonconductive adhesive, the resistor-free side of each ceramic blank could each be bonded to an etched metal lead frame. The

finished component will thus be a "sandwich", with resistor patterns on both outer surfaces of the ceramic and the thin metal lead frame in the middle, as depicted in Figure 68. Connection of this metal inner layer to the logic panel ground plane would create an electrical shield between the two sets of terminator resistors on the outer surfaces of the ceramic and assist in decoupling the internal busses employed in two of the three terminator designs. This design in turn made it feasible to combine the structural advantages of pin-supported

*HIGH-FREQUENCY DOUBLE-SIDED TERMINATOR PACK  
FOR USE WITH SUBNANOSECOND ECL COMPONENTS  
ENCAPSULATED IN LEADLESS CERAMIC CHIP CARRIERS*



ARTIST'S CONCEPTION OF  
NEW MAYO-DESIGNED TERMINATOR PACKS

Figure 68

installation of the terminator packs with solder bonding of resistor contact pads to provide good high frequency performance.

Figure 68, an artist's conception of the terminators, depicts the layout of the internal -2 volt bus (or alternately, the -4.5 volt bus for the "pulldown" packs), which are supplied from contact pads on the ends of the terminator pack; note the positioning of a 3900 pF NPO chip capacitor which decouples the middle of the bus to logic board ground through a center pad. In one type of terminator pack, individual 85 ohm thick film resistors are deposited on the substrate to support the shunt-terminated transmission protocols. In a second type of pack 470 ohm resistors are deposited for use in "pulling down" the source outputs of a differential driving gate. Note that, unlike the design reported in Year 1, both the 85 ohm and the 470 ohm resistor packs will both have on-pack decoupling to ground of the internal busses. As discussed in the Year 1 report, the 470 ohm pull-down resistor packs are not in as serious need of the on-pack decoupling capacitors as are the 85 ohm packs; conversely, the extra decoupling and bus stabilization for the 470 ohm packs may improve system noise margins at high system clock rates. A third terminator pack design provides a group of discrete 100 ohm resistors for connection between the true and complement sides of a differential transmission line. A number of the first terminators manufactured from these

although in any given circuit design the vast majority of chip carrier pads will not require termination (for example, those pads in the middle of a logic string). The required terminator resistors are then connected in a manual operation using a soldering pencil and a solder bridging approach. Hence, the contacts pads for the active resistors in each terminator pack do not extend to the bottom edge of the ceramic substrate, thereby guaranteeing that no inadvertent solder connections will occur during vapor phase reflow bonding of the chip carriers and terminator packs to the logic board. Although a small amount of manual soldering will be required, the number of manual solder bonds will be a very small percentage of the total; the vast majority of bonds will be performed en masse in the vapor phase reflow operation. The use of mechanical installation with the two pins will stabilize the terminator packs during the vapor phase reflow operation.

designs will not be coated with the ceramic overlayer, thereby allowing the components to be installed and tested for performance and noise margins both with and without the on-pack decoupling (as was also done in the Year 1 studies).

All three terminator patterns are designed to require a minimal amount of special preparation of the logic board, such as the cutting of foil traces, regardless of the type of terminator pack installed. The logic board signal layer foils are arranged so that the cutting of a single foil trace at each end of the terminator pack will convert the voltage supplied to the terminator from the usual value, -2 volts, used with the shunt terminators, to -4.5 volts for a "pull-down" resistor pack. However, the supply voltage will always be fed to the terminators through the two end pads regardless of terminator type. The terminator pack containing individual isolated resistors for termination of differential transmission lines does not employ the two end pads at all. Hence, the installation of differential terminator packs requires no special board preparation to insure their proper function.

In the artist's conception of Figure 68, the two end contact pads extend to the bottom of the ceramic substrate (the interface with the logic board) to allow vapor phase reflow bonding to the matching contact pads on the board. With this board and terminator design, it is possible to provide a terminator resistor for every contact pad on the chip carrier,

## SECTION VIII

### REVIEW OF AUTOMATED MANUFACTURING AND TEST EQUIPMENT AND HIGH RESOLUTION COLOR GRAPHICS COMPUTER TERMINALS FOR CAD/CAM

#### 1. Automated Wire Wrap Equipment

An interesting result derived from the Third Engineering Demonstration Test Circuit studies described in the Year 1 Interim Report was the relationship between the numbers and types of errors identified during checkout of this equipment. The Third Demonstration Test Circuit was fabricated using an early version of the subnanosecond ECL CAD/CAM package under development in this project; even at that stage the CAD package was capable of identifying a large percentage of design errors, which could then be corrected prior to board fabrication. During system checkout, a log was maintained of the numbers and types of errors detected, including those attributed to design problems, and those accounted to manufacturing errors.

Approximately 90% of the errors detected in that project were attributed to manufacturing mistakes rather than design problems. Some of these residual design related problems should have been detected by the CAD/CAM program during its verification runs; subsequently, modifications to the CAD/CAM

program were made to detect such errors with a higher degree of confidence. In addition, the 90% of errors which occurred during fabrication consumed much more than 90% of the total time devoted to the correction of all errors from whatever source. This even greater percentage disparity of repair effort for fabrication errors than for design errors is neither surprising nor unusual; design errors can usually be detected during a review of the design documentation; however, almost by definition, there may be no documentation for the fabrication errors.

Based upon these findings, and to improve the overall performance of the Mayo ECL CAD/CAM package, additional software modules have been incorporated into the Mayo CAD/CAM package which allow the preparation of a numerical control tape from the CADED design data base, allowing direct numerically controlled semiautomatic wire wrap fabrication of logic boards. This section will describe our investigation of potentially suitable elements of a computer-aided manufacturing capability, and the project currently underway to verify this CAD/CAM capability through the computer-aided design and fabrication of a small processor.

## 2. Gardiner-Denver & OK Wire and Tool Corporation Semiautomated Wire Wrap Machines

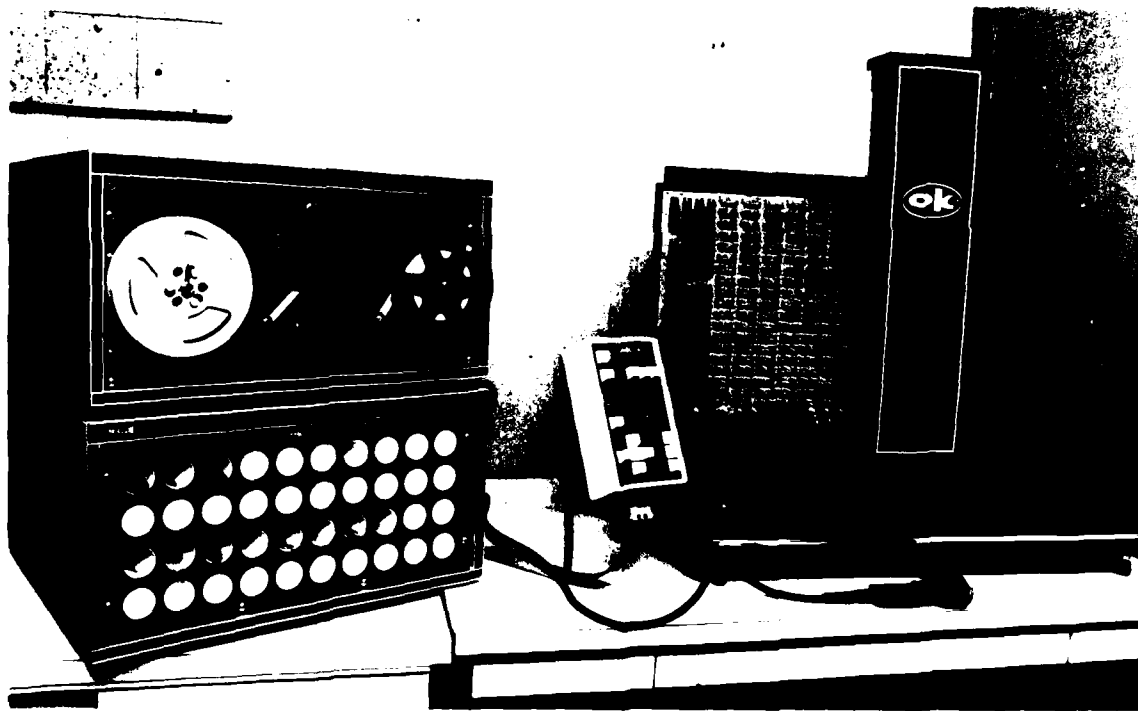
One of the wire wrap machines considered for purchase was the Gardner-Denver SP29 Semiautomatic Wire Wrapping System, which is controlled by a seven-bit punched tape, either in

ASCII or EIA format, at 150 characters per second. Input may be either absolute X-Y positioning, or incremental (relative) positioning. An optional on-line computer control capability is available but was deemed unnecessary for our purposes. The wiring table consists of a moving pointer on a 24" by 38" wiring area, capable of accepting boards up to 26" by 42". The operator rests a conventional wire wrap gun in a tool guide, pushes the wire wrap bit over the pin, and pulls the trigger, thereby completing the wrap. A microswitch on the pointer can be touched with the tip of the gun to advance the machine to the next termination. The pointer moves in increments of .005 inches, at 7.5 inches per second. The entire wiring table is mounted on a free-standing pedestal, equipped with a motor driven vertical adjustment of 19 inches, allowing the board to be raised or lowered to best suit the operator. An optional operator's display console, also driven by the numerical control tape, incorporates most of the same status and prompting functions as the OK Machine and Tool Corporation's SW-101, to be described in the next section. The Gardiner-Denver system also includes a 40-tube wire bin with a digital display to indicate the tube from which to take the proper wire length.

The Gardiner-Denver system was rejected in favor of OK Machine and Tool Corporation's Model SW-101 semiautomated wire wrap machine. The Gardiner-Denver system, with the 40-tube wire bin and a multiformat leader tape kit, lists at \$12,335. The SW-101, with many comparable features, lists at \$4,995,

or approximately 60% less (Figure 69). The Gardner-Denver machine is designed for a heavy production environment rather than for use in a prototype research and development laboratory, and is more rugged than necessary for the latter application. For most system prototyping laboratory environments, the SW-101 should be sufficient.

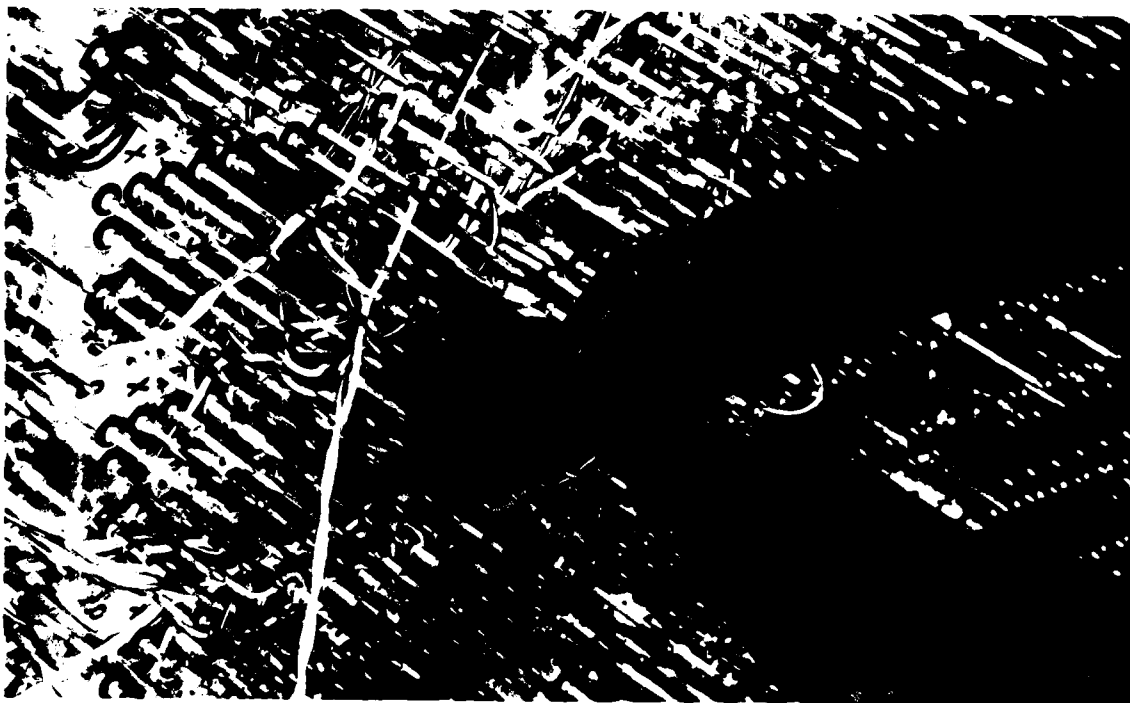
Input for the SW-101 is via seven-bit punched tape, selectable ASCII or EIA, at a rate of 300 characters/second, through a photoelectric, bidirectional spooled tape reader.



OK WIRE AND TOOL CORPORATION MODEL SW-101  
SEMI-AUTOMATIC WIRE WRAP MACHINE

Figure 69

The bidirectional feature permits "backing up" to recheck a wire wrap. Data may be presented either as absolute coordinates (relative to the origin), or incremental (relative to the previous pointer position) coordinates. The wiring table can accommodate boards up to 22" by 30", with an active wiring area of 20 x 20 inches. The unit, which rests on a table top, consists of a moving tool guide which is programmable in increments of .0025 inches, at a rate of 10 inches per second (Figure 70). #7). A microswitch near the tool guide triggers the advance of the tool guide to the next position when touched with bit of the wire wrap gun after completion of the previous wrap.



PHOTOMICROGRAPH OF WIRE WRAP GUIDE OF  
MODEL SW-101 SEMIAUTOMATED WIRE WRAP MACHINE

Figure 70

The controller panel for the SW-101 contains the following functions:

- 1) Control Mode (Operator/Tape) with LED Indicators: In Operator Mode, the operator can control the pointer movements through manual control, and can reset the origin. In Tape Mode, the manual pointer position controls are disabled, and the pointer is under tape control.
- 2) Tape Code (ASCII/EIA) with LED Indicators: This function selects the tape format in operator mode.
- 3) Display Select (Index/X/Y) with LED Indicators and 5 Digit LED Display: This function selects the display to indicate either a sequence number (index), the current X-coordinate, or the current Y-coordinate.
- 4) Parity Error Release, with Parity Error LED and Audible Alarm: In ASCII mode, the input data is checked for even parity. In EIA mode, the input data is checked for odd parity. In either case, if a parity error is detected, the system sounds an alarm, lights the error LED, and halts execution. If the operator depresses the parity error release, execution resumes at the next instruction, assuming that it has no parity error.
- 5) Display Test: This function lights up all LED's to insure that they are working.
- 6) 0,0 Enter/Verify With Check LED: In operator mode, this function is used to reset the origin to the current pointer position. In tape mode, this function forces a return to the origin from the previous position to check for correct

alignment. The function then returns the pointer to its previous position before resuming execution.

- 7) Tape Rewind: In operator mode, this function rewinds the tape to the beginning.
- 8) Tape Forward: This function advances to the next instruction, either by reading from the tape buffer, or by advancing the tape and refilling the internal buffer. This function is also connected to a microswitch on the wiring table.
- 9) Tape Backward: This function allows backstepping one instruction.
- 10) Position Low Speed  $X_{\pm}$ ,  $Y_{\pm}$ : In operator mode, this function advances the pointer at 0.15 ips.
- 11) Position High-Speed Enable: This function increases the above manual rate to 3.5 ips. Note that only under tape control does the pointer advance at a rate of 10 ips.
- 12) Other features include a three-digit display for pin number, a two-digit display for selecting the correct wire bin reference number from the 40-tube wire bin, T1/T2 indicators for first and second termination; finally, eight "directional" LED's indicate the next direction of pointer movement.

One particularly irritating feature of the SW-101 is encountered when, either under tape control or manual (operator) control, the pointer is instructed to move beyond the wiring area. For example, if the pointer is positioned two inches from the top and is instructed to move upward three

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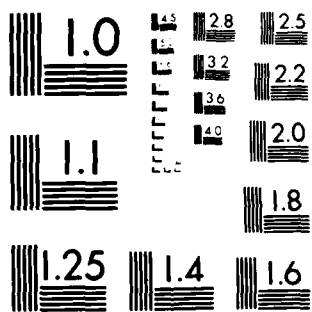
LEADLESS CHIP CARRIER PACKAGING AND CAD/CAM-SUPPORTED  
WIRE WRAP INTERCONN. (U) MAYO CLINIC ROCHESTER MN  
SPECIAL PURPOSE PROCESSOR DEVELOPMEN. B K GILBERT  
NOV 81 AFWAL-TR-81-1206 F33615-79-C-1875 F/G 9/1

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MICROCOPY RESOLUTION TEST CHART  
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inches, the pointer will travel two inches, and, though the pointer can no longer travel any farther, the stepping motors will continue to strain until the machine believes that the pointer has traveled up another inch. Besides placing stress on the motors, this straining continues to advance the X-Y position indicators, although the pointer does not move, until the machine control circuits indicate that it has indeed traveled three inches from its previous location. It is then necessary to recalibrate the 0,0 origin point, as it will be one inch too low. These problems can be circumvented by judicious installation of several microswitches to detect a limit condition. Meanwhile, if one should find the machine grinding against itself, an "Emergency Stop" button is located on the wiring table.

### 3. Verification of Computer-Aided Manufacturing Capability

A design and fabrication project was undertaken to verify correct operation of the CAD/CAM software written in support of the semiautomated wire wrap hardware described above. The project chosen was a redesign of a binary-weighted, nine-element folded convolver-correlator which had been previously fabricated in ECL 100K CERDIP (ceramic dual in-line package) technology, described as the Second Engineering Demonstration Test Vehicle in the Year 1 Interim Report. The redesign was to serve a threefold purpose. First, the task was of a large enough scale, incorporating 118 ECL components, that errors

in the CAD/CAM software not detected in the CADing of smaller test circuits would become apparent and could be corrected. As the response of the convolver-correlator to a given input is already known from previous studies, any deviation from its expected behavior can be detected and traced to the source of the error. Second, since a summer student who is not familiar with the internal mechanism of the CAD/CAM package was assigned the responsibility for the project through the various phases of CADing the design, it would be possible to verify the ease of operator interaction with the CAD in a manner similar to "field testing". Third, this new circuit was designed to stress the maximum operating rate of ECL CERDIP technology in a fully pipelined configuration.

The previously built convolver-correlator was not designed for absolute maximum efficiency. The earlier design was not fully pipelined; several signals must propagate through up to three unclocked devices (e.g., adders) before flowing into a clocked pipeline register, all within a single clock cycle. The propagation delay through these devices becomes nontrivial at high clock rates (100 to 200 MHz). In addition, the pipeline registers used in the earlier design (F100141DC registers) have no complement outputs, a factor which could affect the current flow balance on the -2 V power plane, thereby increasing power plane noise spikes. This earlier convolver-correlator could be made to operate only to a maximum worst case clock rate of 97 MHz.

The redesign incorporates several modifications which should help realize maximum operating speed. Full pipelining has been incorporated into the design by increasing the number of pipeline storage registers from 37 in the old design to 69 in the new circuit. Signals propagate through no more than one unclocked device between clock cycles before arriving at a pipeline register. All pipeline registers used (the F100151DC Hex-D Flip-Flop) have both true and complement outputs, allowing termination of the complement outputs to the -2V power plane and thereby reducing unbalanced loading effects on the -2 volt bus. The new circuit is predicted to run at clock rates of approximately 150 MHz.

As stated earlier, one of the purposes of the fabrication project was to allow a designer unfamiliar with Mayo CAD/CAM package carry a design from: 1) the conceptual phase; 2) through the layout and blueprinting phase; 3) to a generation of the necessary data files for the CAD; 4) execution of the CAD/CAM programs; 5) creation of the wirelist and a CAM tape generated by the programs; 6) operation of the semiautomated wire wrap machine; 7) testing and debugging of the completed circuit; and 8) generation of design changes as necessary using the CAD/CAM software. That portion of this project which had been completed by the end of Year 2 is summarized below.

Corrections to and changes from the previous design were redlined onto a set of blueprints of the prior project. Most

of the changes consisted of adding pipelining registers. A new set of vellums were then prepared and blueprinted. From these blueprints, a data file specifying all the nets was generated as input to the NET module; this module was then executed. Various typographical errors in the data file were flagged and corrected. The BOARD module was executed without incident. A data file for COMP, specifying the components used in the convolver, was created. COMP also executed without detecting any errors.

The physical placement of the ECL components on the board was performed manually, since a new integrated circuit auto-placement routine has been written and tested but not yet integrated into the complete CAD/CAM package. The component assignments were placed in another data file for execution of the ASSIGN module. The CONNECT module also executed without errors. Execution of the VERIFY module detected two errors. One was a design error; a logic high net had a fanout greater than the maximum of fifteen, which was corrected by a redistribution of the loading on the affected logic high nets. The other error was a result of mislabeling the outputs of a chip (mislabeling Q outputs as F outputs). Both errors having been corrected, the modules NET, ASSIGN, CONNECT, and VERIFY were all run again; no additional errors were detected. The last procedure executed was a subordinate section of PROTO, which automatically assigned SIP terminator resistors to all pins needing termination. Work is currently proceeding on the

remainder of PROTO, which will check the interconnect protocols and flag any errors.

By September 1, 1981, the final stages of CAD/CAM generation of the new hardware design should be completed. Specifically, after execution of the PROTO module, the DOCUI module will be integrated and executed, and will list, among other items, certain preparatory steps to ready the circuit board for fabrication. The WIRELST module will generate machine-readable output in the form of punched tape and hard copy printout of the wire wrap connections to be made on the board. After wire wrapping the board under punched tape numerical control, components will be installed and the board tested for logical correctness, and for maximum operational clock rate. Any necessary design changes will be executed via the EC module, thereby completing the project. (Late note: The entire design, automated fabrication, and checkout of this system was completed, ahead of schedule, on August 24, 1981.)

#### Hybrid Technology Corporation Vapor Phase Reflow Solder Machine

A review was undertaken of the offerings of two vendors of vapor phase reflow soldering machines, with eventual elimination from consideration of all but the Phase Four Model 1214 Vapor Phase Soldering System, manufactured by Hybrid Technology Corporation (HTC). The vapor phase soldering process, which uses a heated, inert fluid condensing from its saturated vapor

phase to transfer its latent heat of vaporization to a circuit board, appears to be the most efficient method for soldering leadless chip carriers to circuit boards.

Preparation of the circuit board begins with the application of tiny boli of solder cream to the contact pads of the circuit board. Leadless chip carriers are then emplaced on the board, volatile solvents are driven off, preferably in a low heat oven. The solder cream then acquires a tacky consistency to hold the components in place without the need for other adhesives. The vapor-phase soldering process occurs automatically in several steps. The prepared board, up to 12" by 14" and weighing up to four pounds, is placed horizontally in the basket of an elevator at the top of the unit. The elevator is then lowered into the bottom chamber, which contains the primary working fluid. The bottom chamber contains a heating element which is submerged in and raises the liquid to its boiling point, producing a layer of saturated vapor above the pool of liquid. A primary condensing coil above the vapor layer condenses the vapor for recirculation. The board is carefully lowered into the tank and is brought to rest just above the liquid in the vapor blanket. The working fluid is a fluorinated, nonreactive, organic liquid, Fluorinert FC-70, which boils at 215°C (419°F), slightly higher than the melting point of most tin/lead solders. Thus the temperature of the vapor a constant and equal to the boiling point of the liquid.

The heated vapor condenses on all parts of the board, transferring its latent heat of vaporization quickly (typically 10-30 seconds) to the board, melting and reflowing the solder. The condensed vapor runs off the board and is recirculated.

In the next step, the elevator raises the board past the primary condensing coil into the layer of a secondary vapor blanket consisting of trichlorotrifluoroethane, which has a lower boiling point than that of FC-70. In this secondary layer, any remaining FC-70 condensate is allowed to drain off, and the board is allowed to cool. This layer also prevents the more costly FC-70 gas from escaping into the atmosphere. Finally, the board is raised by the elevator to the top of the unit, completing the process.

#### 5. Leadless Ceramic Chip Carrier Removal Tool

Leadless ceramic chip carriers directly soldered to a circuit board must occasionally be removed and reinstalled, for example, during logic board rework or in the replacement of a defective component. One removal technique involves melting of the solder with a soldering pencil and removing the molten alloy with solder wick. Unfortunately, by the time most of the solder has been removed from one side of the chip carrier and work has begun on the next side, any residual solder from the first side has cooled and hardened; several "passes" are usually required to achieve complete desoldering. An alternate

method uses a high wattage soldering iron to heat the entire chip carrier quickly to the melting point of all the solder contacts; the entire chip carrier is then lifted from the board with a pair of forceps. This removal method may damage the integrated circuit if the heat is excessive. Both methods are relatively inefficient.

A "leadless chip carrier removal tool", the PAK-X-TRAC Model PXT-44A-DM, manufactured by Nu-Concept Computer Systems (as shown in Figure 71) has been purchased and tested. Tip sizes all of which are interchangeable, are available in two categories: under .500", and .500" to 1.3" square. Rectangular tips are also available, and specialized designs will be manufactured upon request. The tips are designed for a minimum clearance between components of .050" at a height of .050" above the board surface for tips greater than .300" square. For tips less than .300", minimum clearance required between components is .035". Modifications for tighter clearances are also available. The model tested has a standard tip of dimensions .400" square.

Removal is accomplished first by anchoring the board. Flux is then applied to the solder fillet points along the edges of the leadless chip carrier. The removal tool is plugged in, and the tips are give time to warm up. The unit is then clamped on the chip, keeping the tips flush with the circuit board. After the solder has melted, the chip may be lifted off the board

while still being held in the tips of the removal tool. The entire process takes little time, does minimal damage to the surface of the circuit board, and is much more efficient than the aforementioned methods of leadless chip carrier removal.

#### 6. Pressurized Viscous Liquid Application Units

The use of vapor phase reflow techniques to solder leadless chip carriers on a circuit board requires placement of a



PAK-X-TRAC LEADLESS CHIP  
CARRIER REMOVAL TOOL

Figure 71

small bolus of solder cream on each contact pad of the circuit board, with each separated from its nearest neighbors by 40 or 50 mils. To assure a good bond, the solder cream deposition process must be reproducible many times with little variance. Manual methods of solder placement have proven unacceptable. A precise, repeatable process utilizes pneumatic dispensing stations for depositing controlled volumes of any liquid or, in this case, high viscosity solder creams.

A Model 200V dispensing system was acquired from the Tridak division of Indicon, Inc. The only services required by the unit are a standard AC line voltage source and a 25-100 p.s.i. air line. A vacuum line may also be attached to exploit a "vacuum pullback", feature, which prevents over-application of low viscosity fluids. The vacuum is also suitable for loading heavy pastes into the dispensing syringes without bubbles. Output pressure is manually adjustable from 0-60 psi, while dispensing time is also manually preset and then initiated by a footswitch. The dispensing duration can be manually controlled, with pressure applied as long as the microswitch is depressed, or can be automatic, in two ranges: .005 to 1.250 seconds, and .010 to 2.500 seconds. The applicators used are disposable polyethylene syringes in 5, 10, or 30 cc sizes. A wide range of needles and tips are available. The so-called "free flow" orifice, which is specially designed for dispensing high viscosity pastes, was tested here (see Figure 67).

An attractive feature of such dispensing systems is the availability of multiorifice manifold nozzles. When a standard design for a given leadless chip carrier has been determined, a custom nozzle can be designed to dispense a controlled bolus of solder cream to each pad simultaneously. This feature would constitute a tremendous time savings, especially when dealing with large leadless chip carriers.

#### Hewlett-Packard 4191A Impedance Measurement Unit

Laboratory verification of the electrical performance of new components necessitates a determination of their impedance characteristics. For example, each contact pad of a leadless chip carrier exhibits parasitic impedance characteristics such as series inductance, in a range of 1-10 nH; shunt capacitance ranging from 0.5 to 5 pF; and series resistance, from 50 to 500 milliohms. For high frequency applications, it is mandatory to evaluate these parameters as a function of frequency, as a basis for comparing different designs of metallization and layer thickness to determine an optimum design for components under development. In general, accurate impedance measurements should be performed at high frequencies and over a wide frequency range, preferably from approximately 50 MHz up to several GHz.

To aid in this effort, a Hewlett Packard 4191A RF Impedance Analyzer has been evaluated for the performance of

direct radio frequency impedance measurements. The unit offers a frequency range of 1 MHz to 1 GHz, with resolution of 100 Hz from 1 to 500 MHz, and 200 Hz from 500 MHz to 1 GHz. The frequency is displayed to seven digits, while the measurement displays (A and B) are accurate to 4 1/2 digits. Error is typically less than 2% of the reading. The unit determines 14 different impedance parameters, all of which are calculated from a single measured complex quantity  $\Gamma$ , the reflection coefficient. A pulse is sent through the device being tested, and the reflection of that pulse is then detected. The reflection coefficient is equal to the complex ratio of the reflected wave voltage to the incident wave voltage. The parameters for display are as follows:

- (a) Impedance, given in polar form with a magnitude,  $|Z|$ , and a phase angle,  $\theta$ , or in rectangular form as resistance,  $R$ , and reactance  $X$ . The usable range for  $\theta$  (in all measurements) is  $\pm .01$  to  $\pm 180$  degrees, while the remaining parameters have a practicable range of 100 milliohms to 20 kilohms.
- (b) Admittance, in polar form as magnitude  $|Y|$  and phase angle  $\theta$ , or in rectangular coordinates with conductance,  $G$ , and susceptance,  $B$ . The usable range of  $G$ ,  $B$ , and  $Y$  is 20  $\mu S$  to 10 S.
- (c) Dissipation factor,  $D$ , and quality factor,  $Q$ , both unitless quantities with a range from .001 to 1000.

- (d) Inductance,  $L$ , with a range of 0.1 nH to 5 mH, and capacitance  $C$  with a range of 0.1 pF to 1  $\mu$ F.
- (e) Reflection coefficient  $\Gamma$ , as previously defined. In polar form, the reflection coefficient is presented as magnitude,  $|\Gamma|$ , and phase angle,  $\theta$ . In rectangular form, the displays show  $\Gamma_x$  and  $\Gamma_y$ . The range is from .000 to  $\pm 1.0000$  for all forms.

The unit also is equipped with an analog X-Y recorder output for direct plotting of measured values versus frequency or measured values versus bias voltage, and has been tested here in this configuration. The HP 4191A is a remarkable device, exhibiting an unprecedented degree of measurement flexibility, programmability, stability, and repeatability. The ease with which it measures the performance of components across a wide range of frequencies makes this unit an almost mandatory acquisition for laboratories involved in the development of high frequency analog or digital systems.

#### 8. Review of Interactive Graphics Terminals Capable of Supporting Computer-Aided Design and Manufacturing

A principle conclusion of the Year 1 development of computer-aided design software was that the entry of initial data into the CAD/CAM package by means of a conventional alphanumeric computer terminal is completely unacceptable. Computer engineers conceptualize their designs in a graphically oriented manner, using block structures and symbolic

notation, to create a traditional "vellum" design. If only alphanumeric data entry into the CAD package is permitted, a traditional paper design must always be generated as the initial task, though the vellum need not contain all detailed design data (such such as component pin numbers) required for the final hardware fabrication. From this engineering drawing, sufficient data is encoded from the blueprint into alphanumeric form via a computer terminal (a task referred to as "yellow-lining" the drawing) to initiate the CAD/CAM program; these first manual steps are tedious, inflexible procedures which interfere with the engineer's desire to perform all design work in graphical form.

The remedy to this problem is the interfacing of a powerful, operator-interactive high resolution graphics terminal to the host computer which supports the CAD/CAM package, and to create the necessary software interfaces between the graphics terminal and the CAD/CAM software package. The designer can then generate a design using MIL-STD-806C electronic logic symbols on the graphics screen.

In brief, it is envisioned that such a CAD graphics terminal in the Mayo laboratories will function as follows. Via light pen or keyboard, the designer accesses a program resident in the microprocessor of the graphics terminal which displays the symbols of the various logic elements available from a library. Components may be selected either with a light pen, a joystick, a trackball, or merely a directional keypad and

cursor. The desired position of the component is indicated in a similar way and the component is embedded into the design. The positioned symbols are connected with lines which represent their electrical connections. Provision should be made to allow editing of the design in the following ways: repositioning of symbols to allow insertion of additional symbols; improvement of the general layout of the design; removal of symbols or lines to change the design; labeling of symbols or lines; retention of a partial design to be completed later; the destruction of an entire section of a design to allow a fresh start. The designer should be able to select from among several sets of symbols representing different types of component technologies or designs. It should also be possible to modify or expand readily any of these logic symbol sets.

As a design is "built up" on the graphics screen, the host computer should be called upon to assemble a large data base which reflects the logical and electrical attributes of the circuit. This data base is then used by the CAD software to apply all of its capabilities to the growing system, including design rule verification, optimized component placement, and interconnect layout; this information can then be returned to the terminal to create a graphical display of the intermediate results, along with error messages if appropriate.

Future uses of a high resolution CAD graphics terminal in the Mayo laboratories will definitely include further graphical

interaction with the CAD software. The CAD packages will be applied to new board designs, new integrated circuit technologies, and will perhaps be expanded to include transistor-level macrocell design of new configurable gate arrays. The terminal will eventually interface with a high-speed plotter to produce logic prints necessary for troubleshooting the actual devices produced.

The search for an appropriate graphics terminal was initiated with a series of utility and feasibility studies using our mainframe computer and an associated Grinnell Corporation 512 x 512 resolution color raster graphics display device normally dedicated to image processing research. A variety of interactive software modules were coded to allow tests of the basic CAD graphics concepts under consideration, for design of the electronic circuits, for physical design of new logic panels, and for component placement on the logic panel. A list of features desirable for such a terminal was then prepared, which included such factors as screen spatial resolution, monochrome versus color display, calligraphic versus raster scan refresh display forms, the amount of local intelligence in and the programmability of the terminal, and mechanisms for communication with a host computer.

All known vendors of graphic terminals addressing the CAD/CAM market were then canvassed for information, literature, and, where possible, live demonstrations. The literature provided

by these vendors was reviewed and compared with the list of desirable features which had been generated.

The list of desired features included a minimum resolution of 1024 x 1024 pixels, allowing a reasonably complex circuit to be erected using recognizable symbols and readable alphanumerics. Color capabilities were desired so that different portions of a circuit could be "highlighted" for easier recognition by the user. High screen writing rate was desired so that the erections of a reasonably complex picture does not require an unacceptable duration. The extra expenditure of funds to gain local processing power would allow a vector to be drawn from a single host command and so that images could be stored in less space. In addition, all systems with a base price exceeding \$50,000 were excluded.

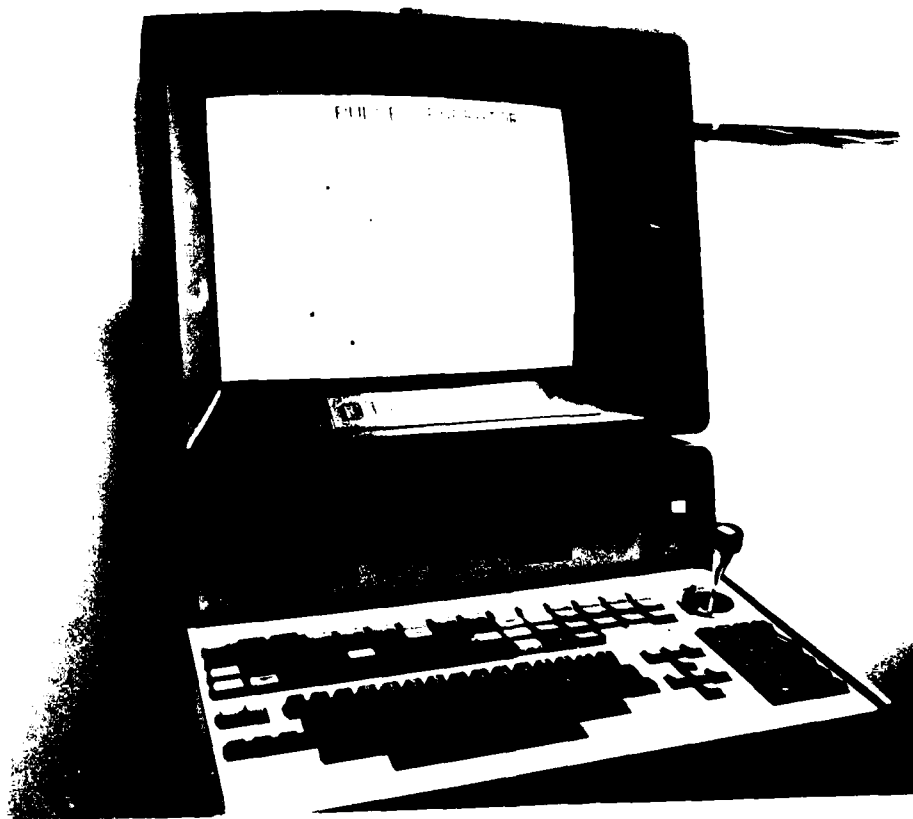
Starting with ten possible vendors, the list was reduced to four companies. A telephone survey of current users of the terminals of each vendor was carried out to ascertain 1) if the terminal companies supported their equipment, 2) the users' reasons for selecting their respective terminals over other candidates, and 3) the types of problems encountered.

At this juncture, the Chromatics Corporation Model CGC 7900 appeared very promising. The Mayo group visited a nearby site with a recently delivered CGC7900 terminal, and expended a day in on on-site trial of the unit. The results of this

test were more positive than could have been expected, particularly regarding the high level of local capability of the terminal. This strong local processing capability allows the CGC 7900 to perform tasks directly for which other terminals require a host computer. The "Plot Mode", which requires no programming by the user, can draw dots, vectors, polygons, circles, arcs, curves, rays, wide vectors, and concatenated vectors, and can also fill in polygons; all of these functions are executable from simple keystroke commands. In "Create Mode", the unit saves keystroke sequences entered by the operator, which can be used later to redraw the picture. Application of these capabilities to our specific needs is apparent. Since the drawing sequences for logic gates and other components can be stored locally in the Chromatics display, the CAD program, resident in the host, can draw a gate by transmitting a single instruction to the CGC 7900 (Figure 72). All of the commands to draw a complete logic schematic can be saved by the Chromatics display on a local hard sectored disc, or in its own semiconductor memory. It is possible to reference, or draw a hard copy, of the schematics from the CGC 7900 without involving the host computer at all.

The CGC 7900 includes, as a standard feature, a Motorola MC68000 microprocessor, which is capable of 8, 16, or 32 bit arithmetic, a stack pointer, 32K bytes of EPROM and 128K bytes of User RAM in its basic version and many additional powerful features. The 24-bit address bus of the M68000 can address

up to 16 megabytes of memory. The CGC 7900 employs a state-of-the-art Mitsubishi 19" Color CRT with a 1024 x 768 pixel resolution. An "overlay" memory plane capable of storing and displaying an alphanumeric array containing 48 lines of 85 characters each. The processor supports 3 types of cursors, graphic plot functions, Pan and Zoom hardware functions which



CHROMATIC CORPORATION MODEL CGC 7900  
HIGH RESOLUTION COMPUTER GRAPHICS TERMINAL

Figure 72

do not affect the contents of the refresh memory, and a "Create buffer" that saves the commands used to generate each picture. Memory refresh is performed by special hardware which also controls memory content modification and two standard serial I/O Ports, allowing fully buffered input and output up to 19.2 K kilobits/second. The above features are all standard equipment.

Our review of the capabilities of the Chromatics 7900 indicated that it was the best unit for the price. An order was placed for a CGC 7900, and the unit has recently been delivered. The optional features ordered also include double density dual-floppy disks with a total of 1 M Byte of storage, an 8" 10 megabyte Winchester fixed disk, a 3 axis joystick, a light pen, 4K of battery backed CMOS RAM to save the state of the terminal when turned off, and 4 bit map memory planes generating 16 simultaneous colors at the full 1024 x 1024 resolution.

## SECTION IX

### SUBNANOSECOND ECL COMPUTER-AIDED DESIGN AND MANUFACTURING SOFTWARE PACKAGE

During the past year, the Mayo Emitter Coupled Logic Computer-Aided Design package (ECL-CAD) has undergone many evolutionary changes; several entirely new capabilities have been incorporated into the software as well. This portion of the Second Interim Report will outline briefly the entire CAD operation, then discuss those portions of the software in which changes and improvements have been made and most of the software preparation effort has been directed; finally, a summary will be presented of the direction of evolution of the entire CAD system.

#### 1. Present CAD Capabilities

A summary of the software modules invoked to "CAD" a design into a functional wire-wrapped circuit is as follows:

- 1) BOARD - defines the wire wrap board configuration and pin labeling;
- 2) COMP - defines a component dictionary which adequately describes each component type required by the design;
- 3) NET - describes the topological intercomponent wire connections to be made during fabrication; however, these connections are tabulated in a manner which

is independent of actual physical layout of components on a logic board;

- 4) ASSIGN - assigns logic components to physical locations on the wire wrap board;
- 5) CONNECT - uses wire-net connection information to connect the physical pins of the wire wrap board;
- 6) VERIFY - applies a set of design rule checks to the connected board;
- 7) TERM - automatically assigns SIP terminator packages to the wire wrap board, and terminates all nets properly according to ECL transmission protocol schemes;
- 8) GROUND - automatically determines ground shielding methods and protocols for each wire net;
- 9) DOCU - generates general documentation listings
- 10) WIRELST - generates a net connection listing and a punched paper tape to drive a semiautomated wire wrap machine;
- 11) TRACE - a terminal-based operator interactive program to aid in operational testing of the completed logic board;
- 12) EC - terminal-based operator interactive program to allow design changes to be made between CAD steps or after an entire CAD run

General improvements have been made to all of the CAD software modules, of which there are more than seventy. Many

of these changes were installed during the conversion of the original version of the CAD/CAM package, which was written for a Control Data CDC-3500 computer, to somewhat different versions for a DEC-10 and Mayo Foundation's new CDC-CYBER 170/720. The major reasons for these changes were: 1) to improve modularity of the entire package; 2) to reduce specific computer dependencies; 3) to localize all remaining machine-specific software dependencies as much as possible; 4) to increase the speed of operation; 5) to reduce machine-specific dependencies on the main data base; and 6) to improve processing of design errors. In addition, a first version of a User's Manual was prepared in early 1981, which provides detailed explanations of the use and operation of the CAD package.

A considerable amount of effort was devoted to the conversion of the CAD package from our older model CDC 3500 computer to the newer DEC 10 and CDC CYBER 170/720 computers. The amount of work necessary to perform these conversions (20 man-weeks) was totally unexpected. The major reasons for this large effort were: 1) different versions of FORTRAN have adopted a wide variety of methods for handling character data; 2) all but the most rudimentary file I/O is nonstandard between different FORTRAN release versions; and 3) the CDC 3500 operating system was extremely outdated with respect to the use of system software utilities, including sorting, text editing, file maintenance, program tape generation, and program listing

generation. This deficiency will be obviated by the conversion to Mayo's new CDC-CYBER 170/720, and the localization of most machine-specific software dependencies.

The addition of data base routines to the CAD/CAM software package has increased overall processing speed, and has allowed the data base to be an independent structure. Input/output functions are now all channeled through one subroutine. Operations such as OPEN, CLOSE, READ, WRITE, CREATE, COPY, and END-FILE are currently supported by the data base subroutines. A paging scheme is now employed in the CAD package whereby individual records are blocked up into larger physical disc records, thus usually reducing the number and duration of disc I/O operations. Paging is now transparent to all of the CAD subroutines. Interactions with individual data records (nodes) or certain collections of these nodes (nets) are handled through two subroutines called NODE and NET, which process all node and net I/O requirements through calls to the CAD package data base I/O routine. These subroutines in effect interact directly with data fields within each node record. The actual structure of each data record is now independent of the characteristics of the CAD operational subroutines, thereby facilitating addition, modification, or removal of data subfields and also permitting packing of fields, which is expected to become necessary in a later stage of software development.

Several of the specific changes that have been made to the CAD software are as follows:

- 1) BOARD - Board location pin groupings are now linked together with a reference pin to facilitate "board tracing";
- 2) COMP - Part type descriptions are included in the component dictionary;
  - component pin logical labels, such as  $C_p$ ,  $Q$ ,  $\bar{Q}$ , etc., are included in the component dictionary, as well as pin numbers;
  - geometric coordinate data in the dictionary is more centralized to facilitate component assignment;
  - component pins are linked to one another through a reference pin to facilitate "component tracing";
  - pins belonging to individual logic elements are linked to one another to facilitate "logic element tracing", and are to be used by future software modules in timing verification and simulation.
- 3) ASSIGN - An assignment subroutine is now used which is also employed by other modules (such as EC and TERM).
- 4) CONNECT - A wire-net source pointer is now included in the connection process to facilitate "net tracing".
- 5) VERIFY - ECL design rules have been rewritten and made more comprehensive to increase their flexibility and generality.

- 6) TERM - This routine has been separated from the VERIFY module so that design rules will be distinct from transmission protocol rules.
- 7) GROUND - This routine has been separated from VERIFY and TERM so that ground shielding is a separate (and optional) process.
- 8) DOCU - This subroutine now directly modifies the data base when board-preparation instructions to the fabrication technicians are generated. This modification was necessary so that the data base will incorporate manual board-preparation operations when engineering changes are made.
- 9) WIRELST - The printout format has been improved;
  - this subroutine now has the capability of generating and verifying a punched paper tape to drive a wire wrap machine.
- 10) TRACE - This subroutine has been given more powerful trace options and more flexible input commands;
  - the subroutine now generates a hard copy listing of trace data when desired.

### 3. Graphics

Throughout most of the year, the addition of hardware-based CAD graphics capabilities to our CAD/CAM software package have been under consideration. An interactive graphics capability is desired for several reasons: 1) it allows the

designer to enter or modify designs more rapidly than by manual paper and pencil methods; 2) data can be abstracted directly from the graphical design by the CAD package, thus eliminating time-consuming and error-prone alphanumeric keyboard entry; and 3) graphic output for board preparation, signal tracing, and system testing is far more effective than printed lists.

The evaluation of a possible CAD graphics capability was directed to two distinct considerations. The first was an evaluation of our requirements for CAD graphics operational features, and a review of the capabilities of commercially available graphics systems. This review is discussed in greater detail in the previous section of this report. The second area of concentration was the performance of a set of experiments during January and February 1981 with raster color graphics on a Grinnell 512 x 512 display already available at Mayo Foundation. These studies were carried out to assist our determination of capability requirements for a CAD graphics terminal, and to investigate the best methods of exploiting the current CAD data base in conjunction with graphical functions.

A preliminary graphics test program was prepared which was capable of extracting graphically useful data from the data base and displaying it under operator interactive control. The user could select the following display options:

- 1) View board pin configurations;
- 2) View board pin grouping configurations;
- 3) View all components assigned to the board;
- 4) View components of a specified part type previously assigned to various board locations;
- 5) View a specified wire net and its connection points;
- 6) View all of the "from" or "to" connections made to a specified component on the board.

The user could also specify color options and scale/offset factors. The subroutine was used to verify a number of hardware and software features which had been suggested for inclusion in candidate color graphics systems.

An expanded version of this graphics function will be installed on our newly purchased Chromatics CGC 7900 1024 x 1024 color raster graphics system, where it will serve as a board preparation, assignment, and debug tool.

#### Current and Future Plans

Currently the Mayo ECL CAD/CAM software package is undergoing an update process in which a variety of new features are being added. An automatic integrated circuit component placement routine has been developed and tested, and is being installed into the package. This capability will allow optimal placement of integrated circuits to minimize total interconnect

wire length; however, the algorithm accepts externally supplied boundary conditions (user specified positions and/or restrictions) and weighting factors to allow the placement of more or less emphasis on specified component assignments and/or connections. This software tool will be a powerful adjunct to the existing CAD package because, unless a design exhibits a high degree of data and signal flow-through, manual placement is a very tedious and subjective process. The auto placement algorithm will in turn be supported by the currently available automatic terminator placement and assignment routines; thus, all components and terminators will be automatically placed.

Timing verification methods are currently under review. The proposed timing verification module will work with gate propagation delays, set-up and hold-times, wire connection lengths, clock frequency, multiphased clocking, and the graphical structure of the design to determine critical timing paths and hazards, assuming a transmission line interconnect environment.

Hierarchical design methods will be applied to the CAD process. The intent of a current project is the installation of a single level of hierarchy, to be exploited through "hardware macro" definitions. This capability will allow the designer to build "macro" structures from "primitives", which in this case are integrated circuit components. The macros

are to be specified as a set of primitives and a set of inter-primitive connections. Once the macro has been defined, it may be employed in the same manner that an integrated circuit is currently used, i.e., it has become a "component".

One deficiency of this "macro method" which immediately becomes apparent is the possible inefficiencies created by the integrated circuits used in the macro. If an integrated circuit section is unused, replication of the macro will increase the number of unused sections. This inefficiency can be eliminated by treating logical elements, rather than entire components, as primitives. It is anticipated that this approach will be attempted following the development of an automatic logic element partitioning routine, also currently under investigation. With this capability, the designer will work entirely with logic elements, and the automatic partitioning routine will assign these logical elements to physical components. This capability will be especially useful when the CAD graphics system is incorporated into the design process.

Other planned projects include: 1) a more refined version of the user documentation, with separate User and Programmer Guides; 2) definitive test cases to be included in the CAD package to verify correct software installation on alternate computer systems; 3) the inclusion of a logic simulation package to work in conjunction with the CAD graphics;

and 4) the extension of the entire CAD package to work with ECL configurable gate arrays, which will be greatly facilitated by the generalization of the previously mentioned design hierarchy concepts.

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